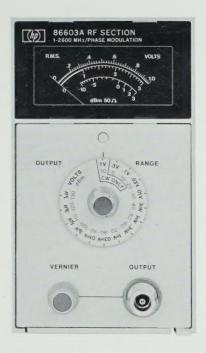
86603A RF SECTION 1-2600 MHz





CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

86603A RF SECTION 1-2600 MHz

Including Options 001, 002, and 003

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed 1921A.

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed 1417A, 1501A, 1505A, 1515A, 1521A, 1533A, 1539A, 1543A, 1550A, 1625A, 1637A, 1638A, 1639A, 1640A, 1653A, 1734A, 1816A, 1834A, and 1847A.

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.



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SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been designed and tested in accordance with international standards.

SAFETY SYMBOLS



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage (refer to Table of Contents).



Indicates hazardous voltages.



Indicates earth (ground) terminal.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND

This plug-in section is used in a Safety Class I product (provided with a protective earthing terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals. Whenever it is likely

that the protection has been impared, the product must be made inoperative and be secured against any unintended operation.

BEFORE CONNECTING THIS SYSTEM TO LINE (MAINS) VOLTAGE

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this system is to be energized via an autotransformer make sure the common terminal is connected to the neutral (grounded side of mains supply). The safety and installation instructions found in Sections II and III of the mainframe should be followed.

SERVICING

WARNINGS

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement in the mainframe.

CAUTIONS

COMPATIBILITY

Damage to the synthesized signal generator system may result if the RF Section is used with unmodified Model 8660A or 8660B mainframes with serial prefixes 1349A and below.



PERFORMANCE TESTING

To avoid the possibility of damage to the instrument or test equipment, read completely through each test before starting it. Then make any preliminary control settings necessary before continuing with the procedure.

PLUG-IN REMOVAL

Before removing the RF Section plug-in from the mainframe, remove the line (Mains) voltage by disconnecting the power cable from the power outlet.

SEMI-RIGID COAX

Slight but repeated bending of the semirigid coaxial cables will damage them very quickly. Bend the cables as little as possible. If necessary, loosen the assembly to release the cable.

FLUX REMOVER

Do not use flux remover anywhere near the A22 assembly. The monoblock capacitors may be damaged by this chemical. If absolutely necessary, use only freon or methanol.

EXPOSED LOW VOLTAGE

The Model 86603A RF Section, when used with early model mainframes, has —32 Vdc exposed on the A20 Assembly and Q1 whenever the mainframe LINE switch is set to STBY. During adjustment and maintenance, do not contact these parts with metal tools. Damage can occur to the mainframe power supply, the A20 Assembly, and/or Q1. Models 8660A and 8660C with serial prefixes 1508A and below, and all 8660B's have this characteristic.



Figure 1-1. HP Model 86603A RF Section (Option 002 Shown)

Model 86603A General Information

SECTION I GENERAL INFORMATION

1-1, INTRODUCTION

- 1-2. This manual contains all information required to install, operate, test, adjust and service the Hewlett-Packard Model 86603A RF Section plugin, also referred to as the RF Section. For information concerning related equipment, such as the Hewlett-Packard Model 8660-series mainframes or the Model 11661 Frequency Extension Module, refer to the appropriate manual or manuals.
- 1-3. This manual is divided into eight sections which provide information as follows:
- a. SECTION I, GENERAL INFORMATION, contains the instrument description and specifications as well as the accessory and recommended test equipment list.
- b. SECTION II, INSTALLATION, contains information relative to receiving inspection, preparation for use, mounting, packing, and shipping.
- c. SECTION III, OPERATION, contains operating instructions for the instrument.
- d. SECTION IV, PERFORMANCE TESTS, contains information required to verify that instrument performance is in accordance with published specifications.
- e. SECTION V, ADJUSTMENTS, contains information required to properly adjust and align the instrument after repair.
- f. SECTION VI, REPLACEABLE PARTS, contains information required to order all replacement parts and assemblies.
- g. SECTION VII, MANUAL CHANGES, contains backdating information to make documentation in this manual applicable to all earlier versions of this instrument.
- h. SECTION VIII, SERVICE, contains descriptions of the circuits, schematic diagrams, parts location diagrams, and troubleshooting procedures to aid the user in maintaining the instrument.

- 1-4. Figure 1-1 shows the Option 002 RF Section.
- 1-5. Packaged with this manual is an Operating Information Supplement. This is simply a copy of the first three sections of this manual. This supplement should stay with the instrument for use by the operator. Additional copies of the Operating Information Supplement may be ordered separately through your nearest Hewlett-Packard office. The part number is listed on the title page of this manual.
- 1-6. On the title page of this manual, below the manual part number, is a "Microfiche" part number. This number may be used to order 4 x 6-inch microfilm transparencies of the manual. Each microfiche contains up to 60 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as all pertinent Service Notes.

1-7. SPECIFICATIONS

1-8. Instrument specifications are listed in Table 1-1. These specifications are the performance standards, or limits against which the instrument may be tested.

1-9. INSTRUMENTS COVERED BY MANUAL

- 1-10. This instrument has a two-part serial number. The first four digits and the letter comprise the serial number prefix. The last five digits form the sequential suffix that is unique to each instrument. The contents of this manual apply directly to instruments having the same serial number prefix(es) as listed under SERIAL NUMBERS on the title page.
- 1-11. For information concerning a serial number prefix not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-12. MANUAL CHANGE SUPPLEMENTS

1-13. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. This unlisted

Table 1-1. Models 86603A/11661 Specifications (1 of 4)

SPECIFICATIONS

FREQUENCY CHARACTERISTICS

Range: 1.0 to 1299.999999 MHz selectable in 1 Hz steps. 1300 to 2599.999998 MHz selectable in 2 Hz steps. Frequencies from 200 kHz to 1 MHz may also be selected with some degradation in specifications.

Accuracy and Stability¹: CW frequency accuracy and long term stability are determined by the aging rate of the time base (internal or external) and its sensitivity to changes in temperature and line voltage. Internal reference oscillator accuracy = \pm aging rate \pm 3 x 10^{-10} /°C \pm 3 x 10^{-10} /1% change in line voltage.

Switching Time: 6 ms to be within 50 Hz of any new frequency selected from 1 to 1300 MHz, 6 ms to be within 100 Hz of any new frequency selected ≥ 1300 MHz. 100 ms to be within 5 Hz of any new frequency selected from 1 to 1300 MHz; 100 ms to be within 10 Hz of any new frequency ≥ 1300 MHz.

Largest Digit Charged	Error at:		
Largest Digit Onargea	1 ms	5 ms	
1 Hz 10 Hz	<1 Hz	<1 Hz	
100 Hz	<100 Hz	<1 Hz	
1 kHz 10 kHz	< 500 Hz	<10 Hz	
100 kHz 1 MHz	< 500 Hz	< 50 Hz	
10 MHz	< 500 Hz	< 50 Hz	
100 MHz, 1 GHz	Undefined	< 50 Hz	

Typical 86603A/11661 Frequency Switching Characteristics (Below 1300 MHz) For center frequencies \geq 1300 MHz, all harmonically related signals are at least 20 dB below the desired output signal for output levels \leq +3 dBm (slightly higher from +3 to +7 dBm).

Sub-Harmonics and Multiples $(\underline{f}, \underline{3f}, \text{etc.})^2$: At center $\underline{2}, \underline{2}$

frequencies \geq 1300 MHz, all sub-harmonics and multiples are at least 20 dB below the desired output signal for output levels \leq +3 dBm (slightly higher from +3 to +7 dBm.)

Spurious Signals (CW, AM and ϕ M only):

At center frequencies < 1300 MHz all non-harmonically related spurious signals are:

- 80 dB down from carrier at frequencies < 700 MHz
- 80 dB down from carrier within 45 MHz of the carrier at frequencies ≥ 700 MHz
- 70 dB down from carrier > 45 MHz from carrier at frequencies \geqslant 700 MHz
- 50 dB down from carrier on the +10 dBm range.
- At center frequencies ≥ 1300 MHz all non-harmonically related spurious signals are:
 - 74 dB down from carrier within 45 MHz of the carrier³.
 - 64 dB down from carrier > 45 MHz from carrier³.

All Power Line Related spurious signals are 70 dB down from carrier at center frequencies < 1300 MHz; 64 dB down ≥ 1300 MHz.

Signal-to-Phase Noise Ratio (CW, AM, and ϕ M only):

Greater than 45 dB in a 30 kHz band centered on the carrier and excluding a 1 Hz band centered on the carrier at center frequencies <1300 MHz; >39 dB in a 30 kHz band centered on the carrier and excluding a 1 Hz band centered on the carrier at center frequencies ≥1300 MHz.

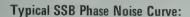
Harmonic Signals: For center frequencies <1300 MHz, all harmonically related signals are at least 30 dB below the desired output signal for output levels ≤+3 dBm; -25 dB for output levels above +3 dBm.

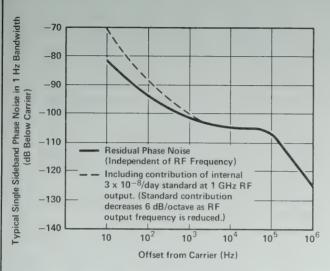
Aging rate for the time base of standard mainframes is 3×10^{-8} /day; for option 001 mainframes, 3×10^{-9} /day.

 $^{^2}$ Below 1300 MHz sub-harmonics and multiples do not exist.

³For output levels +3 dBm and below, slightly higher from +3 to +7 dBm.

Table 1-1. Models 86603A/11661 Specifications (2 of 4)





Typical 86603A Phase Noise Below 1300 MHz (6 dB higher at \geq 1300 MHz)

Signal-to-AM Noise Ratio: Greater than 65 dB in a 30 kHz bandwidth centered on the carrier and excluding a 1 Hz band centered on the carrier.

OUTPUT CHARACTERISTICS

Level: Continuously adjustable from +10 to -136 dBm (0.7 Vrms to 0.03 μ Vrms) into a 50Ω resistive load at center frequencies <1300 MHz; from +7 to -136 dBm (0.5V to 0.03 μ Vrms), into a 50 ohm resistive load at center frequencies ≥ 1300 MHz. Output attenuator calibrated in 10 dB steps from 1.0V full scale (+10 dBm range) to 0.1 μ Vrms full scale (-130 dBm range). Vernier provides continuous adjustment between attenuator ranges. Output level indicated on output level meter calibrated in volts and dBm into 50 ohms.

Accuracy: (Local and remote modes)

±2.5 dB to -76 dBm⁴; ±3.5 dB from -77 to
-136 dBm at meter readings between +3 and
-6 dB.

Flatness: Output level variation with frequency is less than ±2.0 dB from 1-2600 MHz at meter readings between +3 and -6 dB.

Level Switching Time: In the remote mode any level change can be accomplished in less than 50 ms. Any change to another level on the same attenuator range can be accomplished in less than 5 ms.

Impedance: 50Ω .

VSWR: \leq 2.0 on +10 and 0 dBm ranges; \leq 1.3 on -10 dBm range and below.

MODULATION CHARACTERISTICS (With compatible Modulation Sections)

Amplitude Modulation:

Depth: At center frequencies < 1300 MHz, 0 - 90% for RF output level meter readings from +3 to -6 dB and only at +3 dBm and below.

At center frequencies \geq 1300 MHz, 0 - 50% for RF output level meter readings from +3 to -6 dB and only at +3 dBm and below.

AM 3 dB Bandwidth:

Center	AM 3 dB Bandwidth			
Frequency	0 to 30% AM	0 to 70% AM	0 to 90% AM	
<10 MHz	10 kHz	6 kHz	10 kHz	
≥ 10 MHz and				
< 1300 MHz	100 kHz	60 kHz	50 kHz	
≥ 1300 MHz	5 kHz	N/A	N/A	

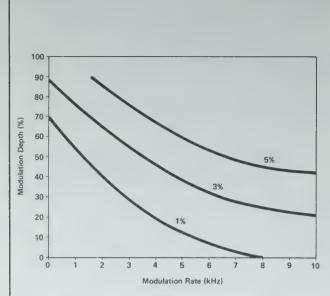
Center	AM Total Harmonic Distortion ⁵			
Frequency	AT 30% AM	AT 70% AM	AT 90% AM	
1-1300 MHz	<1%	<3%	< 5%	
1300- 2600 MHz	< 5%	N/A	N/A	

 $^{^4}$ At frequencies $\geqslant 1300$ MHz, output accuracy and flatness will be slightly degraded at levels from +3 to +7 dBm.

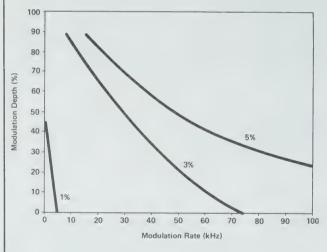
 $^{^5}$ Applies only at 400 Hz and 1 kHz rates with the RF Section front panel meter indicating from 0 to +3 dBm. At a meter indication of -6 dB the distortion approximately doubles. The modulating signal distortion must be <0.3% for the system performance to meet these specifications.

General Information Model 86603A

Table 1-1. Models 86603A/11661 Specifications (3 of 4)



Typical AM Distortion (Center Frequency <10 MHz)



Typical AM Distortion (Center Frequency > 10 MHz but < 1300 MHz)

Incidental PM.

Frequency	Incidental PM
Range	(radians peak at 30% AM)
1-1300 MHz	< 0.2
1300-2600 MHz	< 0.4

Incidental FM:

Frequency Range	Incidental FM (in Hz at 30% AM)
1-1300 MHz	< 0.2 x Fmod
1300-2600 MHz	< 0.4 x Fmod

FREQUENCY MODULATION

Rate: DC to 200 kHz with the 86632B and 86635A. 20 Hz to 100 kHz with the 86633B.

Deviation (peak):

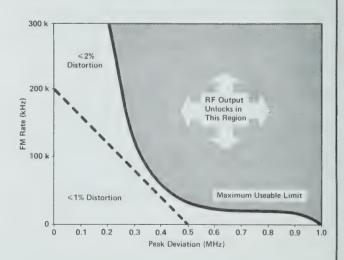
From 1–1300 MHz, 200 kHz-peak with the 86632B and 86635A and 100 kHz-peak with the 86633B. From 1300–2600 MHz, 400 kHz-peak with the 86632B and 86635A and 200 kHz-peak with the 86633B.

Incidental AM: AM sidebands are >60 dB below the carrier with 75 kHz peak deviation at a 1 kHz rate.

Residual FM (FM X0.1 mode): less than 10 Hz-rms in a post detection 300 Hz to 3 kHz band at center frequencies less than 1300 MHz; less than 20 Hz-rms at center frequencies greater than 1300 MHz.

FM Total Harmonic Distortion, (at rates up to 20 kHz):

<1% up to 200 kHz deviation (center frequencies <1300 MHz). <1% up to 400 kHz deviation (center frequencies >1300 MHz). (External modulating signal distortion must be less than 0.3%.)



Typical FM Distortion Curve (< 1300 MHz)

Table 1-1. Models 86603A/11661 Specifications (4 of 4)

PULSE MODULATION (With the 86631B Auxiliary Section only)

Source: External

Rise/Fall Time: 50 ns.

ON/OFF Ratio: At least 40 dB from 1 to 1300 MHz and 60 dB from 1300 to 2600 MHz (with modulation level control at maximum).

Input Level Required: -10 ±0.5 Vdc turns RF on.

PHASE MODULATION (Option 002 Instruments only)

Rate:

With 86635A dc to 1 MHz With 86634A:

dc to 1 MHz at center frequencies less than $100 \ \mathrm{MHz}$

dc to $10\ MHz$ at center frequencies greater or equal to $100\ MHz$.

Maximum Peak Deviation:

0 to 100 degrees peak at center frequencies <1300 MHz. May be overdriven to 2 radians (115°) in Modulation Section external dc mode. 0 to 200 degrees peak at center frequencies ≥1300 MHz. May be overdriven to 4 radians (230°) in Modulation Section external dc mode.

φM Total Harmonic Distortion:

<5% up to 1 MHz rates <7% up to 5 MHz rates <15% up to 10 MHz rates

(External modulation signal distortion must be less than 0.3% to meet this specification.)

REMOTE PROGRAMMING (Through the 8660-series mainframes)

Frequency: Programmable in 1 Hz steps at center frequencies <1300 MHz and in 2 Hz steps from 1300 to 2600 MHz.

Output Level: Programmable in 1 dB steps from +10 to −136 dBm at center frequencies <1300 MHz; +7 to −136 dBm at center frequencies ≥1300 MHz.

Modulation: See specifications for modulation section installed.

GENERAL

Leakage: Meets radiated and conducted limits of MIL-I-6181D.

Size: Plug-in to fit 8660-series mainframe.

Weight: Net 5 kg (11 lb).

General Information Model 86603A

serial prefix indicates that the instrument is different from those documented in this manual. The manual for this instrument is supplied with a yellow Manual Changes supplement that contains "change information" that documents the differences.

1-14. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is keyed to this manual's print date and part number, both of which appear on the title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-15. DESCRIPTION

1-16. The HP Model 86603A RF Section is one of several RF Sections available for use in an 8660-series Synthesized Signal Generator System. This RF Section plug-in is used with an option 100 8660-series mainframe (Frequency Extension Module installed). The RF Section provides precisely tuned RF output frequencies over the 1 to 2600 MHz range with 1 Hz frequency resolution up to 1300 MHz and 2 Hz resolution above 1300 MHz. (8660-series option 004 instruments have resolutions of 100 and 200 Hz respectively.) Frequencies from 200 kHz to 1 MHz can also be generated with some degradation in the amplitude leveling and other related specifications.

1-17. The output power can be set to any level between +10 and -136 dBm (+7 and -136 dBm at center frequencies ≥ 1300 MHz) by means of the front panel VERNIER and calibrated OUTPUT RANGE controls. A front panel-mounted meter and the OUTPUT RANGE switch indicate the output power and voltage levels delivered by the RF Section to any external load having a characteristic impedance of 50 ohms. Output power levels are maintained within ± 2 dB of selected values through internal leveling of the output signal over the full frequency range of the instrument.

1-18. Amplitude, frequency, phase, or pulse modulation of the RF OUTPUT signal can be accomplished within the RF Section by using the appropriate Auxiliary or Modulation Section plug-in.

1-19. External programming permits remote selection of the output signal frequency in 1 or 2 Hz steps (100 or 200 Hz for option 004 mainframes) and the output power in 1 dB steps over the full operating range of the instrument. External programming is accomplished via the mainframe computer-compatible interface and digital control unit circuits.

1-20. OPTIONS

1-21. This RF Section has three options available. They affect the instrument's RF output level, phase modulation, and frequency doubling capabilities.

1-22. Option 001. The RF output attenuator is removed which limits the RF output level range. The output range is +10 to -6 dBm at center frequencies <1300 MHz; +7 to -6 dBm at or above 1300 MHz.

1-23. Option 002. Circuits are added to provide the phase modulation capability. A compatible modulation section is required.

1-24. Option 003. Added circuitry and a switch provides means of front panel control of frequency doubling when the RF Section is used in a mainframe other than a Model 8660C.

1-25. COMPATIBILITY

CAUTION

Damage to the mainframe can result when the RF Section is used with Model 8660A having serial prefix 1349A and below or Model 8660B having serial prefix 1349A and below. To prevent damage install Field Update Kit (08660-60273 or 08660-60274 for 50/400 Hz).

1-26. Many combinations of instruments may be used with the RF Section as part of the Synthesized Signal Generator System. Table 1-2 indicates which RF Section options are compatible to specific mainframes and to the capabilities of the Modulation Sections. Combining option 001 with the types of RF Sections listed does not affect the compatibility.

1-27. The Modulation Sections have various combinations of modulation capabilities depending on the one selected for use with a particular RF Section. In some cases they are partially compatible. For example, when a standard RF Section is installed in an 8660C mainframe along with an FM/ ϕ M Modulation Section, only FM is operable.

Model 86603A

8660A/B^{1,2}

8660C

Modulation Section RF Capabil-**AM** FM Pulse Phase Section ity **Except Options** 8660C (only) 8660C3 8660C NO 002 and/or 003 Option 002 8660C (only) 8660C3 8660C 8660C 8660A/B^{1,2} 8660A/B^{1,2,3} 8660A/B^{1,2} Option 003 NO 8660C 8660C3 8660C

 $8660A/B^{1,2,3}$

8660C3

Table 1-2. Model 86603A RF Section Compatibility

 $8660A/B^{1,2}$

8660C

1-28. EQUIPMENT REQUIRED BUT NOT SUPPLIED

1-29. System Mainframe

Option 002/003

1-30. The mainframe uses phase-locked loops to accurately generate clock, reference, and tuning signals required for operation of the Synthesized Signal Generator System. Front panel-mounted mainframe controls are used to digitally tune two phase-locked loops in the Frequency Extension Module which, in turn, produce high-frequency output signals that are applied to the RF Section. The RF Section mixes the two signals and presents their frequency difference (twice the difference at center frequencies ≥1300 MHz) at the front panel OUTPUT jack. The output frequency is either the value selected by the mainframe front panel controls or externally programmed.

1-31. The mainframe power supply provides all dc operating voltages required by the RF Section, Frequency Extension Module, and Modulation Section plug-ins. Remote programming of the plug-ins is accomplished via the mainframe interface and digital control unit circuits.

1-32. Frequency Extension Module

1-33. The Frequency Extension Module plug-in extends the output frequency range of the mainframe to meet the input requirements of the

RF Section. The Frequency Extension Module plug-in contains two high-frequency phase-locked loops which receive digital tuning signals, variable synthesized signals, and fixed synthesized signals from the mainframe. The phase-locked loops use the mainframe signals, in conjunction with the output frequency from a 4.43 GHz oscillator that is common to both loops, to produce two high-frequency output signals that are supplied to the RF Section. One output signal is generated by a phase-locked loop using a Voltage Controlled Oscillator (VCO) that is tuneable in 1 Hz steps (100 Hz steps for option 004 mainframe) over the 3.95 to 4.05 GHz range. The other output signal is generated by a phase-locked loop using a Yittrium-Iron-Garnet (YIG) oscillator that is tunable in 100 MHz steps over the 3.95 to 2.75 GHz range. The two outputs from the Frequency Extension Module plug-in are applied to the RF Section for mixing, amplification of the converted signal, frequency doubling at center frequencies ≥ 1300 MHz, and final output power level control.

 $8660A/B^{1,2}$

8660C

1-34. Auxiliary Section

1-35. The Auxiliary Section plug-in provides a means of applying externally generated amplitude or pulse modulation drive signals to modulate the RF Section's output carrier.

¹Compatible with new 8660A and 8660B mainframe and modified mainframes of serial prefix 1349A and below. Refer to the paragraph entitled Modification in Section II.

²Compatible with new 8660A and 8660B mainframes and modified mainframes of serial prefix 1503A and below. Refer to the paragraph entitled Modification in Section II.

³Older model Modulation Sections with FM capability will indicate one-half the actual peak FM deviation at center frequencies ≥1300 MHz.

Table 1-3. Test Equipment and Accessories List (2 of 4)

Item	Critical Specifications	Suggested Model	Use*
Connector, BNC Panel Mount		HP 1250-0118	Т
Counter, Computing	50 kHz to 50 MHz with a 1 ms gate time and external trigger; 1 Hz resolution	HP 5360A with HP 5365A plug-in	P
Counter, Frequency	Range 0.2—2600 MHz Resolution 1 Hz 10 MHz external reference output 7.2 Vrms output into 170 ohms	HP 5340A	P
Coupler, Directional	Frequency range 100 MHz to 2.9 GHz	HP 778D Opt. 12	P
Detector, Crystal	1 to 1200 MHz	HP 8471A	P
Detector, Crystal	10 MHz to 2.6 GHz	HP 423A	P, A
Distortion Measurement Set	20 Hz to 20 kHz Capable of measuring <0.1% distortion	HP 339A	P
Filter Kit	Accessory for HP 5210A	HP 10531A	P, A
Filter, Low Pass, 15 kHz	Cut-off frequency 15 kHz	HP 86602-60054 (P/O Kit HP 86602-60050)	P
Filter, Low Pass 4 MHz	Cutoff frequency 4 MHz	CIR-Q-TEL FLT/21B-4-3/50-3A/3B	P
Filter, Low Pass, 2200 MHz	Cutoff frequency 2200 MHz	HP 360C	P
Filters, Low Pass 100 kHz	100 kHz at 50 and 600 ohms	Specials (see Figure 1-2)	A
Filters, Low Pass 1 MHz	1 MHz — 50 and 600 ohms	Specials (see Figure 1-2)	P, A
Filters, Low Pass 5 and 10 MHz	5 and 10 MHz — 50 ohms	Specials (see Figure 1-2)	P
Generator, Pulse	Output — 10 Vpk with ≤10 ns risetime in 600 ohms	HP 8013B	P
Generator, Sweep	Sweep Width 0.1 to 100 MHz Output Level +20 to -80 dBm Flatness ±0.25 dB	HP 8601A	A

Table 1-3. Test Equipment and Accessories List (3 of 4)

Item	Critical Specifications	Suggested Model	Use*
Generator, Synthesized Signal	±1 Hz from 1 MHz to 1300 MHz ±2 Hz from 1300 to 2600 MHz +7 dBm output 10 MHz Reference Frequency output >0.5V into 170 ohms	HP 8660C with HP 86631B and HP 86603A plug-ins	P, A
Mixer, Double Balanced	1 MHz to 110 MHz	HP 10514A	A
Mixer, Double Balanced	300 to 2000 MHz	Watkins-Johnson MIJ	P
Oscillator, Test	1 kHz to 10 MHz 1.0 to 2.0 Vrms into 600 or 50 ohms Distortion less than 0.3%	HP 651B	P, A
Oscilloscope	Vertical: Bandwidth 50 MHz with sensitivity of 5 mV/ division minimum Horizontal: Sweep time 10 ns to 1 s Delayed sweep External triggering to 100 MHz	HP 180C with HP 1801A and HP 1821A plug-ins	P, A,
Oscilloscope, 10:1 divider probes	10:1 divider, input impedance 10 megohm shunted by 10 pF	HP 10004	P, A,
Power Meter/Sensor	Range: -10 to +10 dBm from 10 MHz to 2.6 GHz	HP 435A/8481A	P, A,
Power Supply, DC	0-10 volts	HP 6215A	P
Programmer, Marked Card	Capable of programming BCD or HP-IB data	HP 3260A Opt 001	P, A
Probe, Logic	TTL compatible	HP.10525T	Т
Resistor, 1000 ohm	±2%	HP 0757-0280	Р, А
Resistor, 10K ohm	±2%	HP 0757-0442	P
Resistor, 100K ohm	±2%	HP 0698-7284	P
Service Kit	Interconnect cables, adapters, and coaxial cables compatible to 8660-series plus and jacks	HP 11672A (See Operating Note or mainframe manual for parts list)	А, Т
Stub, Adjustable	Frequency range 100 MHz to 2.0 GHz	General Radio 874-D50L	Р

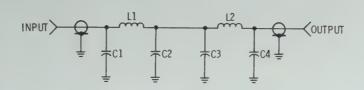
Table 1-3. Test Equipment and Accessories List (4 of 4)

Item	Critical Specifications	Suggested Model	Use*
Tee, Coaxial	2 required	HP 1250-0781 (BNC)	P,A
Termination, 50 ohm Feedthru	50 ohm	HP 11048C	P
Termination, 50 ohm	50 ohm (2 required)	HP 11593A	P
Test Set, Phase Modulation	Input Frequency Range 250 to 450 MHz Distortion <2.0% up to 2 MHz rates <3.5% up to 5 MHz <5.0% up to 10 MHz	HP 8660C-K10 (only)	P
Voltmeter, AC	Accuracy ±2% of full scale from 1 Hz to 1 MHz 1 mVrms to 10 Vrms full scale	HP 403B	P, A, 7
Voltmeter, Digital	Range 0.00 to 60.00 volts DC Accuracy ± (0.3% of reading +0.01% of range) AC Accuracy ± (0.25% of reading +0.05% of range) 45 Hz to 20 kHz	HP 3466A	P, A, 7

^{*}Use: P = Performance Tests, A = Adjustments, T = Troubleshooting

Model 86603A General Information

LOW PASS FILTERS



100 kHz - 50 ohms

100 kHz - 600 ohms

C1, C4 0.015 μ F Myler	0160-0194	C1, C4	1300 pF	0160-2221
C2 $0.027 \mu F Myler$	0170-0066	C2	3000 pF	0160-2229
C3 $0.022 \mu F Myler$	0160-0162	C3	1100 pF	0160-2219
L1, L2 100 μ H	9140-0210	L1, L2	$1200~\mu H$	9100-1655

1 MHz - 50 ohms

1 MHz - 600 ohms

C1, C4	1500 pF	0160-2222	C1, C4	130 pF	0140-0195
C2	3300 pF	0160-2230	C2	300 pF	0160-2207
C3	1600 pF	0160-2223	C3	110 pF	0140-0194
L1, L2	$10~\mu H \pm 10\%$	9140-0114	L1, L2	$120 \mu H$	9100-1637

5 MHz - 50 ohms

10	MHz	 50	ohms	

C1, C2, C4	300 pF	0160-2207	C1, C4	150 pF	0140-0196
C3	680 pF	0160-3537	C2	330 pF	0160-2208
L1, L2	$2 \mu H$	9100-3345	C3	160 pF	0160-2206
			L1, L2	1 µH ±10%	9140-0096

NOTE

Unless otherwise noted, tolerance of components is $\pm 5\%$ and capacitors are mica. Part numbers are Hewlett-Packard.

Figure 1-2. Low Pass Filters



SECTION II INSTALLATION

2-1. INTRODUCTION

2-2. This section provides information relative to initial inspection, preparation for use, and storage and shipment of the Model 86603A RF Section plug-in. Initial Inspection provides instructions to be followed when an instrument is received in a damaged condition. Preparation For Use gives all interconnection necessary and installation instructions. Storage and Shipment provides instructions and environmental limitations pertaining to instrument storage. Also provided are packing and packaging instructions which should be followed in preparing the instrument for shipment.

2-3. INITIAL INSPECTION

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in Figure 1-1, and procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the electrical performance test, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection.

2-5. PREPARATION FOR USE

2-6. Power Requirements

2-7. All power required for operation of the RF Section is furnished by the mainframe. This RF Section requires approximately 50 volt-amperes.

2-8. Interconnections

2-9. Prior to installing the RF Section plug-in into the mainframe, verify that the Frequency Extension Module plug-in and interconnecting cable assemblies have been installed in accordance with the instructions contained in the Frequency Extension Module manual.

2-10. Rear Panel Test Switch Setting

2-11. Before inserting the RF Section into the mainframe, set the rear panel Frequency Doubler Test Switch to the proper position. When used with the Model 8660C mainframe, the switch is set to the 8660C position. When used with Models 8660A or 8660B (option 003), the switch is set to 8660A/B. With options other than 003, the switch is set to 8660A/B X1 or X2.

2-12. Modifications

2-13. Modifications to older versions of Model 8660A and 8660B mainframes are required if they are to be used with the RF Section.

CAUTION

Damage to the synthesized signal generator system may result if the RF Section is used with an older unmodified Model 8660A or 8660B mainframe.

2-14. Power Supply Modification. Due to the increased power consumption of the RF Section in the doubled mode and/or with the phase modulation option, the Model 8660A and 8660B mainframes with serial prefixes 1349A and below must be modified by installing a Field Update Kit. For mainframe configurations other than option 003 (60 Hz line operation), order kit number 08660-60273. For option 003 mainframes (50-400 Hz line operation) order kit number 08660-60274.

NOTE

Verify that a new higher current fuse, HP Part Number 2110-0365, 4A, Slow Blow, is used in mainframes with the power supply modification.

2-15. Frequency Doubler Function Modification. To ensure proper operation of the frequency doubler function of option 003 RF Sections, a

Field Update Kit must be installed in Model 8660A and 8660B mainframes of serial prefix 1503A and below. For mainframe configurations other than option 005 (BCD programming format), order kit number 08660-60306. For option 005 mainframes (HP-IB format), order kit number 08660-60308.

2-16. Operating Environment

2-17. The RF Section is designed to operate within the following environmental conditions:

Temperature	۰						٠			$\dots 0^{\circ} \text{ to } +55^{\circ}\text{C}$
Humidity			 ٠	۰	۰	٠	٠	۰		less than 95%, relative
Altitude								۰	٠	. less than 15,000 feet

2-18. Installation Instructions

WARNING

The multi-pin connector which provides interconnection from mainframe to RF Section, will be exposed with the RF Section removed from the right-hand mainframe cavity. With the Line (Mains) Voltage off and power cord disconnected, power supply voltages may still remain which, if contacted, may constitute a shock hazard.

2-19. Insert the plug-in approximately half-way into the right cavity of the mainframe. Rotate the latch (lower right corner) to the left until it protrudes perpendicular to the front panel. Refer to Figure 2-1, which shows the plug-in partially inserted into the mainframe and the latch rotated to a position that is perpendicular to the plug-in front panel. Push the plug-in all the way into the mainframe cavity and then rotate the latch to the right until it snaps into position.

2-20. STORAGE AND SHIPMENT

2-21. Environment

2-22. The storage and shipping environment of the RF Section should not exceed the following limits:

Temperature	 	 	$\dots 140^{\circ}$ to $+75^{\circ}$ C
Humidity	 	 	less than 95%, relative
Altitude	 	 	. less than 25,000 feet

2-23. Packaging

2-24. Original Type Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to assure careful handling. In any correspondence refer to the instrument by model number and full serial number.

- **2-25.** Other Packaging. The following general instructions should be used for re-packaging with commercially available materials:
- a. Wrap the instrument in heavy paper or plastic. (If shipping to a Hewlett-Packard office or service center, attach a tag indicating the type of service required, return address, model number, and full serial number.)
- b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.
- c. Use enough shock-absorbing material (3 to 4-inch layer) around all the sides of the instrument to provide firm cushion and prevent movement inside the container. Protect the control panel with cardboard.
 - d. Seal the shipping container securely.
- e. Mark the shipping container FRAGILE to assure careful handling.

Model 86603A Installation



Figure 2-1. RF Section Partially Inserted into Mainframe



SECTION III OPERATION

3-1. INTRODUCTION

3-2. This section contains information which will enable the operator to learn to operate and quickly check for proper operation of the RF Section plug-in as part of the Synthesized Signal Generator System.

3-3. PANEL FEATURES

3-4. The front and rear panel controls, connectors, and indicators of the RF Section and its options are described by Figure 3-1, 3-2, and 3-3.

3-5. OPERATOR'S CHECKS

3-6. The RF Section, as part of the Synthesized Signal Generator System, accepts inputs from the rest of the system but controls only the RF Output level. Even though the controlled circuits for most other functions are within the RF Section, the actual checks are found in the manual of the instrument which controls that function.

3-7. The Operator's Checks in this manual are intended to verify proper operation of the circuits which control and are controlled by the RF output level controls. This includes the meter, the

VERNIER control, the OUTPUT RANGE switch, and the Output Range Attenuator when operating in the local mode. When the system is being remotely controlled, the 1 dB and 10 dB remote step attenuator switches are checked in place of the VERNIER control and OUTPUT RANGE switch. Refer to Figure 3-4.

3-8. OPERATING INSTRUCTIONS

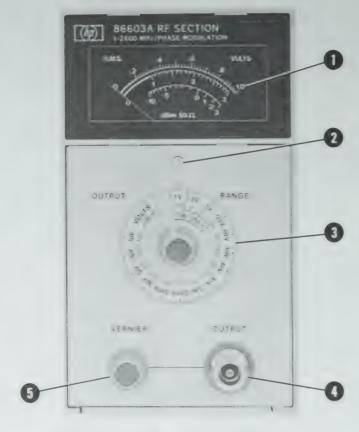
3-9. In this system, the mainframe and plug-ins contain the controls for frequency, modulation, and RF level selection. The mainframe controls frequency, the Modulation Section plug-in controls modulation type and level, and the RF Section plug-in controls RF output level. The Operating Instructions for the RF Section plug-in are included in Table 3-1.

3-10. OPERATOR'S MAINTENANCE (Option 003 Only)

3-11. Maintenance responsibility for Option 003 RF Sections consists of changing the FREQ DOUBLER indicator lamp if it burns out. The lens is turned counterclockwise until it can be removed and the defective lamp is removed and discarded. The lamp HP part number is 2140-0092.

FRONT PANEL FEATURES

86603A EXCEPT OPTION 003

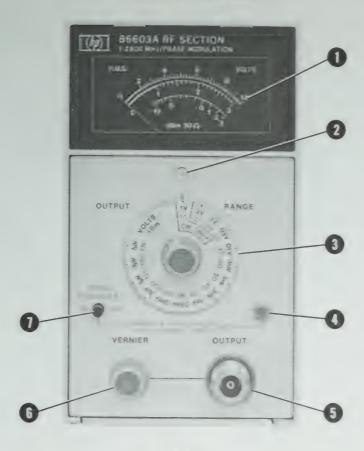


NOTE

The front panel of the option 002 instrument is shown. The standard instrument does not have the term PHASE MODULATION after 1–2600 MHz. The option 001 instrument has an OUTPUT RANGE switch which shows only the +10 and 0 dBm ranges.

- 1 Meter. Indicates the RF output level in Vrms and dBm (50Ω) with the scale reference indicated by the OUTPUT RANGE switch.
- 2 Mechanical Meter Zero Control. Sets the panel meter indicator to zero when the Mainframe LINE switch is set to STBY.
- 3 OUTPUT RANGE Switch. Sets the output level range of all except option 001 instruments from +10 to $-130~\mathrm{dBm}~(50\Omega)$ in 10 dB steps. For option 001 instruments, +10 and 0 dBm ranges only.
- OUTPUT Jack. Type-N female coaxial connector. RF output level +10 to -136 dBm (0.7 Vrms to 0.03 μ Vrms) at center frequencies <1300 MHz; +7 to -136 dBm (0.5 Vrms to 0.03 μ Vrms) at \geq 1300 MHz.
- **5** VERNIER Control. RF output continuously variable within the useable range (+3 to -6 dB) as indicated by the meter.

FRONT PANEL FEATURES 86603A OPTION 003



NOTE

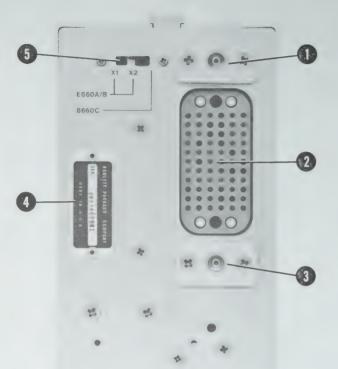
The front panel of the option 002/003 instrument is shown. The option 003 instrument does not have the term PHASE MODULATION after 1-2600 MHz. The option 001/003 has an OUTPUT RANGE switch which shows only the +10 and 0 dBm ranges.

- **Meter.** Indicates the RF output level in Vrms and dBm (50Ω) with scale reference indicated by the OUTPUT RANGE switch
- 2 Mechanical Meter Zero Control. Sets the panel meter indicator to zero when the Mainframe LINE switch is set to STBY.
- 3 OUTPUT RANGE Switch. Sets the output level range of all except option 001/003 instruments from +10 to -130 dBm (50Ω) in 10 dB steps. For option 001 003, +10 and 0 dBm ranges only.
- FREQ DOUBLER Lamp. Lamp is illuminated when the output frequency is doubled (≥1300 MHz) in Model 8660A or 8660B mainframes.

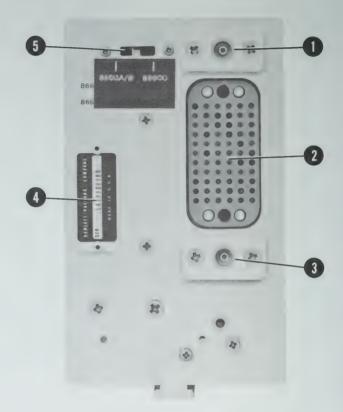
- 5 OUTPUT Jack. Type-N female coaxial connector. RF output level to +10 to −136 dBm (0.7 Vrms to 0.03 μVrms) at center frequencies ≤1300 MHz; +7 to −136 dBm (0.5 Vrms to 0.03 μVrms) at ≥1300 MHz.
- 6 VERNIER Control. RF output continuously variable within the useable range (+3 to -6 dB) as indicated by the meter.
- FREQ DOUBLER Switch. Controls frequency doubling capability from the front panel. This function is performed automatically when the RF Section is used with an 8660C mainframe or in 8660A and 8660B mainframes in the remote mode.

REAR PANEL FEATURES

86603A EXCEPT OPTION 003

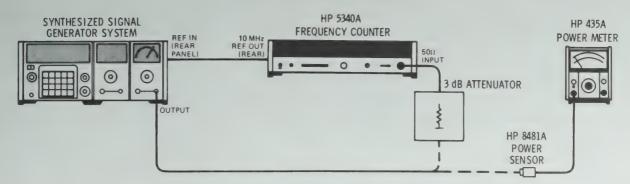


86603A OPTION 003



- 1 Coaxial Plug. Connects the 3.95 to 2.75 GHz RF Input signal to the RF Section from the Frequency Extension Module.
- 2 Interconnect Plug. Provides interconnection of power supply voltages; RF and control signals between the RF Section plug-in and the mainframe, Frequency Extension Module, and Modulation Section plug-in.
- 3 Coaxial Plug. Connects the 3.95 to 4.05 GHz LO Input signal to the RF Section plug-in from the Frequency Extension Module.
- 4 Serial Number Plate. Metal plate with stamped serial number. Four-digit and letter for prefix. Suffix is unique to an instrument.
- Frequency Doubler Test Switch. Primary use is for testing RF Section operation in various mainframes. Set to 8660C position when used with 8660C mainframes. For instruments other than option 003, the 8660A/B X1 and X2 positions are to be used for test purposes only. For option 003 instruments, set the switch to the 8660A/B position when used with 8660A or 8660B mainframes.

OPERATOR'S CHECKS



WARNING

BEFORE CONNECTING THIS SYSTEM TO LINE (MAINS) VOLTAGE, the safety and installation instructions found in Sections II and III of the mainframe manual should be followed.

CAUTION

Damage to the signal generator system may occur if the RF Section is used with unmodified 8660A and 8660B mainframe with serial prefix 1349A and below. See the paragraph entitled Power Supply Modification in Section II.

NOTE

Refer to the paragraphs entitled Compatibility (Section I), and Rear Panel Test Switch Setting and Installation (Section II).

1. Set the System controls as follows:

Mainframe:

LINE Switch	٠					۰		0	o	ON
REFERENCE SELECTOR							۰		a	EXT
CENTER FREQUENCY.		۰	0		۰			٠		500 MHz
Cootion Dlania										

Modulation Section Plug-in:

MODE Switch OFF

RF Section Plug-in:

OUTPUT RANGE Switch 0 dBm

VERNIER Control +3 dB meter reading

- 2. Connect the RF Section OUTPUT to the power sensor input. Verify that the amplitude of the 500 MHz signal is approximately +3 dBm.
- 3. Set the OUTPUT RANGE Switch to +10 dBm and adjust the VERNIER control for a —3 dB reading. Verify that the output level is approximately +7 dBm.

OPERATOR'S CHECKS

- 4. Connect the RF Section OUTPUT to the frequency counter input through the 3 dB attenuator. Verify that the output frequency is 500.000 000 MHz plus or minus one count.
- 5. Set the Signal Generator System center frequency to 1400 MHz. For 8660A or 8660B mainframes (Option 003 RF Section) set the center frequency to 700 MHz and press the RF Section FREQ DOUBLER switch. Verify that the front panel X2 lamp is illuminated and the frequency output is 1400 MHz.

NOTE

Programming center frequencies ≥1300 MHz is not possible with unmodified Model 8660A and 8660B mainframes of serial prefix 1503A and below. Refer to paragraph entitled Frequency Doubler Function Modification in Section II.

6. To check the remote control capabilities of the RF Section, connect a control unit to the mainframe. Repeat steps 1 through 5 while the system is remotely programmed from the external source. Application Note 164-1 "Programming the 8660A/B Synthesized Signal Generator" provides the information needed for remote BCD operation of this system. Application Note 164-2 "Calculator Control of the 8660A/B/C Synthesized Signal Generator" provides the information needed for calculator control of the system using the HP-IB (option 005). Section III of the mainframe manual contains the same information in abridged form.

NOTE

For 8660A and 8660B mainframes, entry into the frequency doubling mode is not automatic and therefore must be programmed. To program center frequencies less than 1300 MHz, program the center frequency, the center frequency address, and the X1 frequency range address. To program center frequencies \geq 1300 MHz, program exactly one-half the desired center frequency, the center frequency address, and the X2 frequency range address.

Frequency Range Addresses

Center Frequency	BCD	HP-IB
Range	Address	Address
<1300 MHz (X1)	9 (1001)	I
≥1300 MHz (X2)	7 (0111)	G

Table 3-1. Operating Instructions (1 of 2)

OPERATING INSTRUCTIONS

TURN ON

WARNING

BEFORE CONNECTING THIS SYSTEM TO THE LINE (MAINS) VOLTAGE, the safety and installation instructions found in Sections II and III of the mainframe manual should be followed.

CAUTION

Damage to the signal generator system may occur if the RF Section is used with an unmodified 8660A and 8660B mainframe of serial prefix 1349A and below. See the paragraph entitled Power Supply Modification in Section II.

NOTE

Refer to the paragraphs entitled Compatibility (Section I) and Rear Panel Test Switch Setting and Installation (Section II)

1. On the mainframe front panel, set the LINE switch to ON; on the rear panel, set the REFER-ENCE SELECTOR switch to INT. Wait for the mainframe "oven" indicator to go out.

FREQUENCY SELECTION

- 2. Refer to Section III of the mainframe operating and service manual for information on system frequency selection.
 - a. When used with 8660C mainframes, the RF Section's rear panel Frequency Doubler Test Switch should always remain in the 8660C position.
 - b. The desired frequency range must be selected if the RF Section is used with the 8660A or 8660B mainframes. The RF Section's Frequency Doubler Test Switch should be set to the 8660A/B position.
 - (1) For center frequencies <1300 MHz, the front panel FREQ DOUBLER switch should be pressed and released and the front panel FREQ DOUBLER lamp should be off.
 - (2) For center frequencies ≥1300 MHz, the front panel FREQ DOUBLER switch is pressed and the FREQ DOUBLER lamp should be illuminated. The selected center frequency must be exactly half the desired center frequency.

RF OUTPUT LEVEL

3. DBM. Set the OUTPUT RANGE switch to within +3 and -6 dB of the desired output level. Adjust the VERNIER control for a meter reading which when added to the OUTPUT RANGE switch indication equals the desired output level.

PERFORMANCE TESTS

4-9. FREQUENCY RANGE

SPECIFICATION:

1 to 1299.99999 MHz selectable in 1 Hz steps; 1300 to 2599.999998 MHz selectable in 2 Hz steps. Frequencies from 200 kHz to 1 MHz may also be selected with some degradation in specifications.

DESCRIPTION:

The Synthesized Signal Generator System RF OUTPUT is monitored by a frequency counter which supplies a common time base reference signal. The frequencies are checked at the extremes. Any specified frequency may be checked.

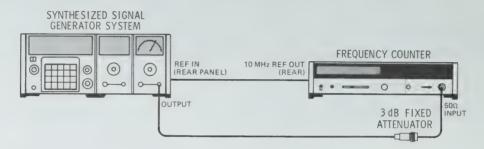


Figure 4-1. Frequency Range Test Setup

EQUIPMENT:

NOTE

In the following procedure, allow for accuracy of counter used. Model recommended is specified at ± 1 count.

- 1. Connect frequency counter 10 MHz output reference signal to mainframe EXT REF input as shown in Figure 4-1 and set mainframe rear panel REF switch to EXT.
- 2. Set the RF Section OUTPUT RANGE switch to 0 dBm; set the VERNIER control full CW.
- 3. Set mainframe center frequency to 1.000000 MHz and check RF section output frequency with counter. Record the frequency.

0.999999	1	Λ	\cap	ባበ	01	7	V/I	П	P2
0.000000		. U	w	w	UJ		VI.		1

4. Set mainframe center frequency to 1299.999999 MHz (Option 004 mainframe set to 1299.9999 MHz) and check RF Section output frequency with counter. Record the frequency.

1299.999998	_1300.000000 MHz
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5. Set mainframe center frequency to 2599.999998 MHz (Option 004 mainframe set to 2599.9998 MHz) and check RF Section output frequency with the counter. Record the frequency.

2599.999997 2599.99	999	999	MHz
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PERFORMANCE TESTS

4-10. FREQUENCY ACCURACY AND STABILITY

SPECIFICATION:

CW frequency accuracy and long term stability are determined by, the aging rate of the time base (internal or external) and its sensitivity to changes in temperature and line voltage. Internal reference oscillator accuracy = \pm aging rate $\pm 3 \times 10^{-10}$ /° C $\pm 3 \times 10^{-10}$ /1% change in line voltage. (Aging rate for the time base in the standard mainframe is 3×10^{-8} /day; for option 001 mainframes, 3×10^{-9} / day.)

NOTE

If there is any reason to doubt the mainframe crystal oscillator accuracy or stability, refer to the performance test in Section IV of the mainframe manual.

4-11. FREQUENCY SWITCHING TIME

SPECIFICATION:

6 ms to be within 50 Hz of any new frequency selected up to 1300 MHz, 6 ms to be within 100 Hz of any new frequency selected \geq 1300 MHz. 100 ms to be within 5 Hz of any new frequency selected up to 1300 MHz; 100 ms to be within 10 Hz of any new frequency selected \geq 1300 MHz.

DESCRIPTION:

A change in the Synthesized Signal Generator System's frequency is remotely programmed; after a preset time interval the frequency is measured. A trigger pulse from the programming device is first coupled to the oscilloscope. The pulse is delayed a preset interval by the oscilloscope and then coupled to the computing counter at which time the frequency is measured.

NOTE

The frequencies were selected for worst-case conditions (longest switching time). Due to the frequency doubling circuits, the equivalent worst-case conditions above 1300 MHz will produce exactly twice the frequency deviation for the specified switching time.

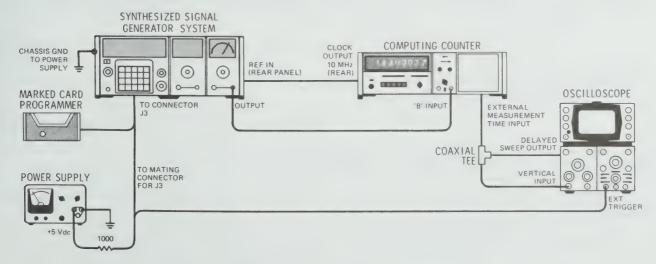


Figure 4-2. Frequency Switching Time Test Setup

PERFORMANCE TESTS

4-11. FREQUENCY SWITCHING TIME (Cont'd)

EQUIPMENT:

 DC Power Supply
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PROCEDURE:

- 1. Connect the dc power supply +5 volt output through a 1000 ohm resistor to pin 17 of the mating connector for J3. Pin 17 (flag) of the Marked Card Programmer output connector is also connected to the oscilloscope ext trigger input.
- 2. Connect the marked card programmer to mainframe rear panel connector J3.
- 3. Connect oscilloscope delayed sweep output through a BNC TEE to oscilloscope channel A vertical input and to computing counter rear panel external time measurement input.
- 4. Set counter controls as follows: rear panel switch to trigger; "B" channel to X1 sensitivity; module switch pressed; digits displayed for necessary resolution; measurement time to 1; counter gate time to 1 ms.
- 5. Program the System for 19.999999 MHz. Set the mainframe rear panel reference switch to external.
- 6. Set oscilloscope controls as follows: trigger to ac slow; ext, negative slope, trigger level at about 9:00 o'clock; sweep mode auto; delay trigger auto; main sweep 1 ms; delay sweep 0.1 µs; main sweep mode.
- 7. Set oscilloscope trace to start at left vertical graticule line. Use oscilloscope delay control to delay spike 5.5 divisions from CRT left graticule line.
- 8. Switch oscilloscope sweep mode from auto to normal.
- 9. Program the system for 30.000000 MHz. Frequency displayed on computing counter should be 30 MHz \pm 50 Hz. Record the frequency.

29.999950______30.000050 MHz

10. Program the system for 29.999999 MHz. Frequency displayed on counter should again be within ± 50 Hz of programmed frequency.

29.999949______30.000049 MHz

- 11. Set Oscilloscope normal sweep for 10 ms and delay sweep to 1 μ s.
- 12. Set Oscilloscope sweep mode to auto and delay control for a delay spike 9.5 divisions from the CRT left graticule line.
- 13. Set Oscilloscope main trigger to normal and computing counter gate time to 10 ms.

4-11. FREQUENCY SWITCHING TIME (Cont'd)

14. Program the System for 30.000000 MHz. Frequency displayed on computing counter should be within ± 5 Hz of programmed frequency.

29.999995______30.000005 MHz

15. Program the System for 29.999999 MHz. Frequency Displayed on computing counter should be within ± 5 Hz of programmed frequency.

29.999994______30.000004 MHz

NOTE

To reduce the effect of random errors, steps 5 through 10 and 13 through 15 may be repeated several times (5 minimum). Record the average frequency.

4-12. OUTPUT LEVEL SWITCHING TIME

SPECIFICATION:

In remote mode, any level change can be accomplished in less than 50 ms. Any change to another level on the same attenuator range can be accomplished in 5 ms.

DESCRIPTION:

The Synthesized Signal Generator System RF OUTPUT level (attenuation) is remotely programmed while the RF OUTPUT is detected and monitored by an oscilloscope. Because the oscilloscope is triggered by the programming device, the time needed to effect the level change may be measured directly on the oscilloscope CRT.

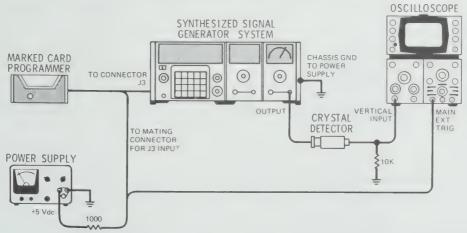


Figure 4-3. Output Level Switching Time Test Setup

EQUIPMENT:

 Marked Card Programmer
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4-12. OUTPUT LEVEL SWITCHING TIME (Cont'd)

PROCEDURE:

- 1. Connect equipment as illustrated in Figure 4-3. Note that +5 volt output from DC Power Supply is connected through a 1000 ohm resistor to pin 17 of mating connector to J3 and to Oscilloscope external trigger input.
- 2. Connect RF Section OUTPUT through crystal detector to oscilloscope Channel A input.
- 3. Set Oscilloscope controls as follows: Main Time/Div, 5 ms; Vertical input, dc coupled, 0.2 V/Div; Normal Sweep; Ext Trigger, negative slope, AC slow, Trigger level about 9:00 o'clock.
- 4. Program the System's center frequency for 500 MHz and 10 dB attenuation of the RF output signal. Reprogram for 19 dB attenuation. Switching time should be less than 5 ms. Record switching time.

10 to 19 dB5	ms
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5. Program the RF Section attenuation for 10 dB, then for 30 dB. Switching time should be less than 50 ms.

10 to 30 dB_____50 ms

6. Repeat steps 4 and 5 with center frequency set to 1 MHz.

10 to 19 dB_____5 ms

7. Repeat step 4 with the center frequency set to 2599 MHz.

10 to 19 dB______5 ms

4-13A. OUTPUT ACCURACY

SPECIFICATIONS:

 ± 2.5 dB to -76 dBm; ± 3.5 dB to -136 dBm. (Maximum specified levels +10 dBm at center frequencies <1300 MHz; +3 dBm with slightly degraded accuracy from +3 to +7 dBm, at center frequencies ≥ 1300 MHz.)

DESCRIPTION:

The RF level accuracy for the +10 and 0 dBm ranges is measured with a power meter. For the lower ranges, an IF substitution measurement technique is used.

RF level (attenuation) measurements using IF substitution is accomplished by 1) converting the RF output to a low frequency IF signal, 2) offsetting the decrease in RF level (increase in attenuation) by an equal decrease in IF attenuation. This maintains a fairly constant output level at the IF load. The intermediate frequency is selected on the basis of availability of a precision attenuator. Therefore, any variation in output level from an established reference is primarily due to the RF attenuator.

4-13A. OUTPUT ACCURACY (Cont'd)

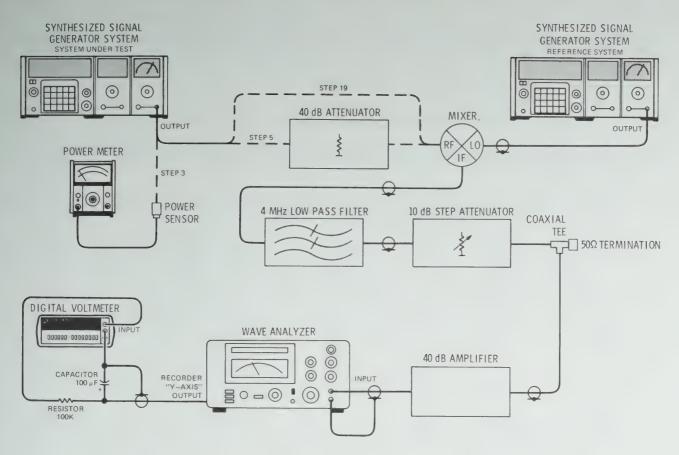


Figure 4-4A. Output Accuracy Test Setup

EQUIPMENT:

Power Meter/Sensor	
Synthesized Signal Generator HP 8660C/86603A/86631B	
40 dB Attenuator	
Mixer Watkins-Johnson M1J	
4 MHz Low Pass Filter CIRC-Q-TEL FLT/21B-	
4-3/50-3A/3B	
Coaxial Tee (BNC)	
50 Ohm Termination HP 11593A	
40 dB Amplifier	
Double Shielded Cables (5-required) HP 08708-6033	
Capacitor	
Resistor	
Type N-to-SMA Adapter OSM 21040	
SMA-to-OSM Right Angle Adapter OSM 219	
SMA-to-BNC Adapter (2) OSM 21190	
10 dB Step Attenuator	
Wave Analyzer HP 3581A	
Digital Voltmeter HP 3466A	

4-13A. OUTPUT ACCURACY (Cont'd)

PROCEDURE:

- 1. Set the System Under Test Controls for a center frequency of 2000.000000 MHz and an output level of +10 dBm.
- 2. Set the power meter controls for the +15 dBm range.
- 3. Connect the power sensor to the RF Section OUTPUT jack of the System Under Test.
- 4. Set the RF Section controls as shown in the table below and verify that the RF output level is within the specified tolerance.

Synthesized Signal G	D		
OUTPUT RANGE Switch (dBm)	Panel Meter Reading (dB)	Power Meter Reading (dBm)	
+10*	0	+7.5+12.5	
+10*	-3	+4.5+ 9.5	
+10*	6	+1.5+ 6.5	
0	6	-8.5 - 3.1	
0	-3	-5.5 - 0.5	
0	0	-2.5+ 2.5	
0	+3	+0.5+ 5.5	

NOTE

Be careful not to vary the RF Section's VERNIER control setting throughout the rest of this procedure.

- 5. Connect the 40 dB attenuator directly to the OUTPUT jack of the RF Section in place of the power sensor.
- 6. Connect the "R" port of the mixer directly to the 40 dB attenuator using the Type N-to-SMA adapter and the SMA-to-OSM right angle adapter.
- 7. Connect the 4 MHz Low Pass Filter to the "I" port of the mixer with a SMA-to-BNC adapter.
- 8. Connect the cable from the Reference System output to the "L" port of the mixer with a SMA-to-BNC adapter.

NOTE

Be sure all connections are tight to prevent RF leakage

9. Set the reference system controls for a center frequency of 2000.011000 and an output level of +7 dBm. Set the rear panel reference selector to external.

4-13A. OUTPUT ACCURACY (Cont'd)

- 10. Set the 10 dB Step Attenuator to 50 dB.
- 11. Set the wave analyzer controls as follows: frequency 11 kHz, resolution bandwidth 3 Hz, sweep mode off, $dBv/LIN-dBm\ 600\Omega$ switch to dBv/LIN, amplitude reference level $-40\ dB$, AFC switch unlock and scale 10 dB.
- 12. Connect the other equipment which follows the 4 MHz Low Pass Filter as shown in Figure 4-4A.
- 13. Tune the wave analyzer frequency control for the maximum meter reading. Adjust the input sensitivity and vernier controls for a midscale meter reading. Press the AFC control for frequency lock.
- 14. Wait 30 seconds for the DVM reading to stabilize. Record the DVM reading. This is the reference level equivalent to the last power meter reading (\approx +3 dBm).
- 15. Use the following formula to calculate the obsolute RF output level from the System Under Test:

 $dBm = dBm_1 - \triangle dB + 2(V-V_{ref})$

dBm is the RF output level

 dBm_1 is the actual RF level measured at the +3 dBm (0 dBm OUTPUT RANGE setting) in Step 4. ΔdB is the difference in 10 dB step attenuator setting.

V is the DVM reading for each individual OUTPUT RANGE. Vref is the reference DVM reading.

NOTE

The wave analyzer recorder output sensitivity is 2 dB/volt.

16. Set the RF Section OUTPUT RANGE switch to -10 dBm; Set the 10 dB step attenuator to 40 dB. Wait 30 seconds for the reading to stabilize. Record the DVM reading in the table following step 17. Calculate and record the RF level in the table.

Example:
$$dBm = dBm_1 - (\triangle dB) + 2 (V_1 - V_{ref})$$

 $dBm_1 = 2.8 dBm$
 $\triangle dB = 10 dB$
 $V_1 = 2.388 Vdc$
 $V_{ref} = 2.433 Vdc (from step 14)$
 $dBm = 2.8 - (10) + 2(2.388 - 2.433)$
 $= 2.8 - 10 + 2(-0.045)$
 $= -7.29 dBm$

17. Continue as in step 16, to measure, record and calculate the DVM reading and RF level for each OUTPUT RANGE Setting as shown in the following table.

4-13A. OUTPUT ACCURACY (Cont'd)

OUTPUT RANGE	10 dB Step Attenuator	DVM Reading	Ak	Absolute RF Outp Level (dBm)	
Switch (dBm)	(dB)	(Vdc)	Min.	Actual	Max.
0 -10 -20 -30 -40 -50	50 40 30 20 10		$ \begin{array}{r} + 0.5 \\ - 9.5 \\ -19.5 \\ -29.5 \\ -39.5 \\ -49.5 \end{array} $		$\begin{array}{c} + 5.5 \\ - 4.5 \\ -14.5 \\ -24.5 \\ -34.5 \\ -44.5 \end{array}$

- 18. Set the 10 dB step attenuator to 50 dB.
- 19. Remove the 40 dB attenuator and connect the mixer directly to the OUTPUT jack of the system under test.
- 20. Increase the wave analyzer's input sensitivity by 10 dB. If necessary, adjust the input sensitivity vernier for a midscale meter reading.
- 21. Transfer the last calculated RF output level on the preceding table to the first line on the following table. Wait 30 seconds and record the new DVM reading.
- 22. Use the formula and the new V_{ref} level to calculate the RF level for each range shown in the table.

OUTPUT RANGE	10 dB Step Attenuator	DVM Reading	Absolute RF Output Level (dBm)		out
Switch (dBm)	(dB)	(Vdc)	Min.	Actual	Max.
-50	50		-49.5		-44.5
-60	40		-59.5		-54.5
-70	30		-69.5		-64.5
-80	20		-80.5		-73.5
-90	10		-90.5		-83.5
-100	0		-100.5		-93.5

- 23. Set the wave analyzer's AFC switch to unlock (off). Adjust the frequency control for the peak reading equal to the last recorded DVM reading on the previous table.
- 24. Set the 10 dB step attenuator to 30 dB.
- 25. Set the wave analyzer amplitude reference level to -60 dB. Increase the input sensitivity 10 dB.
- 26. Transfer the last RF output level reading on the preceding table to the first line of the following table. After 30 seconds record the new DVM reference on the first line of the following table.

4-13A. OUTPUT ACCURACY (Cont'd)

27. Measure, calculate, and record the DVM reading and RF level for each OUTPUT RANGE Setting as shown in the following table. Due to the high noise levels evident on this test, there is appreciable deviation in the wave analyzer and DVM readings. Record the average reading.

OUTPUT RANGE	10 dB Step Attenuator	DVM Reading	At	put	
Switch (dBm)	(dB) (Vdc)		Min.	Actual	Max.
-100 -110 -120 -130	30 20 10 0		-100.5 -110.5 -120.5 -130.5		- 93.5 -103.5 -113.5 -123.5

NOTE

Output level accuracy may be checked at any frequency between 300 and 2000 MHz using this procedure. This procedure may also be used at the frequency extremes if a well shielded mixer specified for the desired frequency range is used in place of the Watkins-Johnson M1J.

4-13B. OUTPUT ACCURACY - ALTERNATE PROCEDURE

SPECIFICATION:

 ± 2.5 dB to -76 dBm; ± 3.5 dB to -136 dBm. (Maximum specified levels ± 10 dBm at center frequencies ± 1300 MHz; ± 3 dBm with slightly degraded accuracy from ± 3 to ± 7 dBm, at center frequencies ± 1300 MHz.)

DESCRIPTION:

The RF level Accuracy for the +10 and 0 dBm ranges is measured with a power meter. A reference level is established and accuracy is checked from 0 dBm to -80 dBm by comparing the RF Section attenuation against a calibrated 10 dB step attenuator.

NOTE

This procedure checks all sections of the RF Section Attenuator separately. Also, the 10 dB, 20 dB, and 40 dB sections are checked in all possible combinations. The sum of the -70 dBm inaccuracy and the change in accuracy at -80 dBm shall not exceed ± 1.0 dB.

4-13B. OUTPUT ACCURACY - ALTERNATE PROCEDURE (Cont'd)

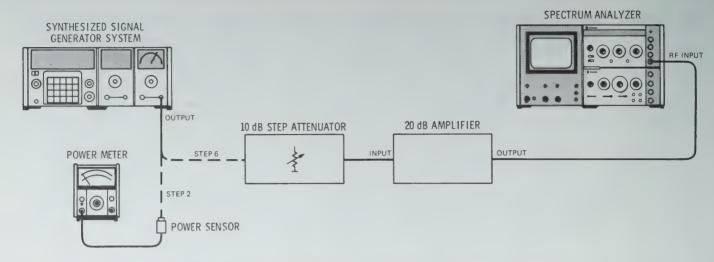


Figure 4-4B. Output Accuracy Test Setup (Alternate Procedure)

EQUIPMENT:

PROCEDURE:

- 1. Set the system controls for a frequency of 30 MHz and an output level of +10 dBm.
- 2. Connect the power sensor to the RF Section's OUTPUT jack.
- 3. Set the RF Output Level as shown in the table below and verify that the level is within the specified tolerance.

Synthesized Signal COUTPUT RANGE Switch (dBm)	Power Meter Reading (dBm)	
110*	0	+7.5 +12.5
+10*	0	
+10*	-3	+4.5+ 9.5
+10*	-6	+1.5+ 6.5
0	-6	_8.5
0	-3	-5.5 0.5
0	0	-2.5+ 2.5
0	+3	+0.5+ 5.5

NOTE

Do not change the RF Section VERNIER control setting until this procedure is completed.

4-13B. OUTPUT ACCURACY - ALTERNATE PROCEDURE (Cont'd)

- 4. Set the spectrum analyzer controls as follows: center frequency 30 MHz, frequency span per division 5 kHz, resolution bandwidth 3 kHz, input attenuation 10 dB, vertical sensitivity per division 2 dB, and sweep time per division 5 ms.
- 5. Set the 10 dB Step attenuator switch to 80 dB.
- 6. Connect the equipment as shown in Figure 4-4B.
- 7. Adjust the reference level range and vernier to establish a reference level on the analyzer display.
- 8. On the first line of the following table, record the power meter reading shown on the preceding table for the OUTPUT RANGE setting of 0 dBm and the panel meter reading of +3 dB. This is the absolute RF level which corresponds to the display reference.
- 9. Set the OUTPUT RANGE switch and the 10 dB Step Attenuator range switch settings as shown on each line of the following table. Record the display variation from the established reference.
- 10. Calculate the RF level using the following formula:

 $dBm = dBm^1 - \Delta dB_{10} + \Delta dB$

dBm is the RF output level

dBm¹ is the RF level measured at +3 dBm (0 dBm OUTPUT RANGE setting) in step 3.

 ΔdB_{10} is the change in 10 dB Step Attenuator level

∆dB is the variation from the established display reference for each OUTPUT RANGE setting.

For example, results of the first step are:

 $dBm_1 = +2.8$

 $\Delta dB_{10} = 10$

 $\Delta dB = -0.2$

dBm = +2.8 dBm -10 dB + (-0.2) dB

= -7.4 dBm

10 dB Step Attenuator	•	RF Output Level (dBm)		
(dB)	Min.	Measured	Max.	
80 70 60 50 40 30 20	+ 0.5 - 9.5 -19.5 -29.5 -39.5 -49.5 -59.5		+5.5 -4.5 -14.5 -24.5 -34.5 -44.5 -54.5 -64.5	
20 10 0	-59.5 -69.5 -80.5			

11. Subtract the two levels obtained for OUTPUT RANGES of -70 and -80 dBm. The level change should be 10 ± 1 dB.

9 dB______11 dB

4-14. OUTPUT FLATNESS

SPECIFICATION:

Output level variation with frequency is less than ± 2.0 dB from 1-2600 MHz. (Applicable at the following RF levels: ± 10 to ± 136 dBm at center frequencies ± 1300 MHz; ± 3 to ± 136 dBm with slight degradation in flatness from ± 3 to ± 7 dBm at center frequencies ± 1300 MHz.)

DESCRIPTION:

After an output level reference is established, power level measurements are made at various frequencies across the range of the Synthesized Signal Generator System. The output levels must fall within the limits specified.

EQUIPMENT:

Power Meter/Sensor HP 435A/8481A

PROCEDURE:

- 1. Zero the Power Meter.
- 2. Set the system center frequency to 1500 MHz.
- 3. Set the Power Meter range switch to 0 dBm; set the RF Section OUTPUT RANGE Switch and VERNIER Control for an output level of -2.0 dBm as read on the power meter.
- 4. Measure and record the power level indicated by the Power Meter at the following center frequencies: 1 MHz, 10 MHz, 100 MHz, 500 MHz, 1000 MHz, 1299 MHz, 2000 MHz, and 2599 MHz.

1 MHz	-4.0	0.0 dBm
10 MHz	-4.0	0.0 dBm
100 MHz	-4.0	0.0 dBm
500 MHz	-4.0	0.0 dBm
1000 MHz	-4.0	0.0 dBm
1299 MHz	-4.0	0.0 dBm
2000 MHz	-4.0	0.0 dBm
2599 MHz	-4.0	0.0 dBm

4-15. HARMONIC SIGNALS, SUB-HARMONIC, AND SUB-HARMONIC MULTIPLES

SPECIFICATION:

For center frequencies <1300 MHz, all harmonically related signals are at least 30 dB below the desired output signal for output levels $\leq+3$ dBm.)(-25 dB for output levels above +3 dBm.)

At or above 1300 MHz, all harmonically related signals are at least 20 dB below the desired output signal for levels \leq +3 dBm (slightly higher from +3 to +7 dBm.)

At center frequencies ≥1300 MHz, all sub-harmonics and multiples are at least 20 dB below the desired output signal for output signals ≤+3 dBm. (Slightly higher from +3 to 7 dBm.)

NOTE

Below 1300 MHz sub-harmonics and multiples do not exist.

4-15. HARMONIC SIGNALS, SUB-HARMONIC, AND SUB-HARMONIC MULTIPLES (Cont'd)

D	m	Q	\sim	\mathbf{p}	Т	D	П	т	റ	N	T	۰
v	<u>uv</u>	D	\mathbf{c}	T	'n	Ł	щ	т	v	7	u	۰

A spectrum analyzer is used to measure the relative levels of the second and third carrier hard	monics and
the sub-harmonics and their multiples with respect to the carrier fundamental at various cent	er frequencies.

EQU	JIPMENT:										
	Spectrum Analyzer	8555A/8552B/14	T0:								
PRC	OCEDURE:										
1.	Set the system center frequency to 1299 MHz; set the RF Section VERNIER control for an output level of +10 dBm.	OUTPUT RANGE	switch and								
2.	Connect the power meter/sensor to the system RF OUTPUT jack.										
3.	Readjust the VERNIER control for a power meter reading of +10 of	dBm.									
4.	Set the spectrum analyzer input attenuation to 30 dB. Connect the spectrum analyzer RF input.	RF Section OUTF	PUT jack to the								
5.	Set the other spectrum analyzer controls for convenient viewing of necessary to view the second and third harmonics. Record the harmonical signal.										
		Secon	d Third								
	1299 MHz ≥25	dB down									
6.	Repeat steps 1 through 5 at the other frequencies listed. Record th	e levels.									
		Secon	d Third								
	1000 MHz ≥25										
	500 MHz ≥25										
	$ \begin{array}{rcl} 100 \text{ MHz} & \geqslant 25 \text{ o} \\ 10 \text{ MHz} & \geqslant 25 \text{ o} \end{array} $										
7.	Set the system center frequency to 100 MHz; set the RF Section O and the VERNIER control for a front panel meter reading of +3 dB										
		Secon	d Third								
	100 MHz ≥30 c	dB down									
8.	Set the system center frequency to 1400 MHz.										
9.	Adjust spectrum analyzer controls to display the carrier. Readjust third harmonics. The harmonic signals should be ≥ 20 dB down with										
	1400 MHz ≥20 c	Secon	d Third								
10.	Set the system center frequency to 2500 MHz. Repeat step 8 and r	ecord the signal lev	vels.								
		Secon	d Third								
	2500 MHz ≥20 c	dB down									

4-15. HARMONIC SIGNALS, SUB-HARMONIC, AND SUB-HARMONIC MULTIPLES (Cont'd)

11. Set the system's fundamental (center) frequency as shown in the table. Adjust the spectrum analyzer controls to display the sub-harmonics and their multiples. Set the RF Section VERNIER control for a panel meter reading of −6 dB when measuring the f/2 sub-harmonics and +3 dB when measuring the 3f/2 sub-harmonics. These signals should be ≥20 dB down from the fundamental.

Fundamental	Sub-Harmo	nic Multiples
(f in MHz)	(f/2 in MHz)	(3f/2 in MHz)
1400 2500	700 1250	2100 3750

		f/2	3f/2
1300 MHz	>20 dB down		
2500 MHz	>20 dB down		

4-16. PULSE MODULATION RISETIME

SPECIFICATION:

50 nanoseconds.

DESCRIPTION:

The external pulse generator output is coupled to the RF Section plug-in through the Model 86631B Auxiliary Section. The pulse modulated signal is detected and the rise time measured with an oscilloscope.

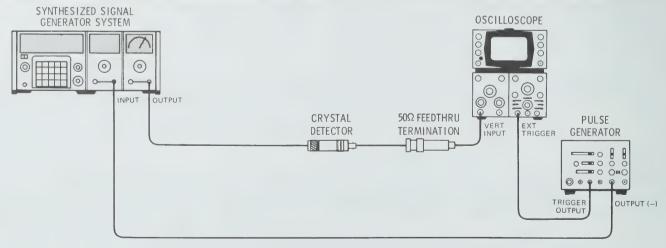


Figure 4-5. Pulse Modulation Risetime Test Setup

EQUIPMENT:

4-16. PULSE MODULATION RISETIME (Cont'd)

PROCEDURE:

- 1. Set System center frequency to 1200 MHz.
- 2. Set the RF Section OUTPUT RANGE switch and VERNIER control for an output of +10 dBm.
- 3. Set the Auxiliary Section external modulation switch to pulse; set pulse level control full cw.
- 4. Adjust pulse generator output for -10 Vpk (into 50Ω) with risetime $\leq 10 \text{ ns}$; set pulse repetition rate and width to convenient values.
- 5. Connect equipment as illustrated in Figure 4-5.
- 6. Adjust oscilloscope to display leading edge of detected pulse modulated RF signal. Risetime, as measured between the 10% and 90% amplitude points on leading edge, should be 50 nanoseconds or less.

		50	n

4-17. PULSE MODULATION ON/OFF RATIO

SPECIFICATION:

At least 40 dB for center frequencies <1300 MHz; at least 60 dB for center frequencies ≥1300 MHz.

DESCRIPTION:

An HP Model 86631B Auxiliary Section is inserted in the left cavity of the mainframe. A dc level of —9.5 Vdc (pulse-on) and 0.0 Vdc (pulse-off) is applied to the Auxiliary Section. The RF output of the system is monitored on a spectrum analyzer. The ratio of the pulse-on to pulse-off level is the on-off ratio.

EQUIPMENT:

- 1. Set System center frequency to 500 MHz, RF Section OUTPUT RANGE switch and VERNIER control for an output level +10 dBm, and Auxiliary Section external modulation switch to PULSE.
- 2. Set the spectrum analyzer input attenuation to 30 dB; connect the RF Section OUTPUT to the analyzer RF input.
- 3. Connect -9.5 Vdc from the power supply to the Auxiliary Section input.
- 4. Adjust the analyzer controls for a CRT display of the carrier. Establish the reference by positioning the carrier peak on the top horizontal graticule line.
- 5. Set the power supply output to 0.0 Vdc. Set the Pulse Level control fully clockwise. The signal displayed should be >40 dB down from the reference.

40 dB	down
-------	------

4-17. PULSE MODULATION ON/OFF RATIO (Cont'd)

6. Set the System center frequency to 2000 MHz. Repeat steps 3 through 5 and record the RF level. The level should be down >60 dB.

60 dB	down	

4-18. AMPLITUDE MODULATION DEPTH AND 3 dB BANDWIDTH

SPECIFICATION:

Depth: At center frequencies <1300 MHz, 0-90% for RF output meter readings from +3 to -6 dB and only at +3 dBm and below.

Rate: At center frequencies < 10 MHz

10 kHz from 0-30% AM

6 kHz from 0-70% AM

5 kHz from 0-90% AM

At center frequencies ≥10 to <1300 MHz

100 kHz from 0-30% AM

60 kHz from 0-70% AM

50 kHz from 0-90% AM

At center frequencies ≥1300 MHz

5 kHz from 0-50% AM

NOTE

To check AM accuracy, refer to Section IV of the appropriate Modulation Section Operating and Service Manual.

DESCRIPTION:

The system RF output is amplitude modulated. The signal is demodulated by a peak detector in a spectrum analyzer (the frequency-span width is set to zero). The ac and dc components are measured with a voltmeter at the detector (vertical) output. First, the dc component is set to -283 mVdc plus a detector offset correction. Then, the ac component is measured. The AM level (%) is 1/2 (one half) the rms output.

Because of the required measurement accuracy, the accuracy of the spectrum analyzer's detector offset must be known to ± 2 mVdc. The offset voltage is calculated by measuring the change in the detector output for a change in the RF input and assuming a linear detector over the range of the levels used.

4-18. AMPLITUDE MODULATION DEPTH AND 3 dB BANDWIDTH (Cont'd)

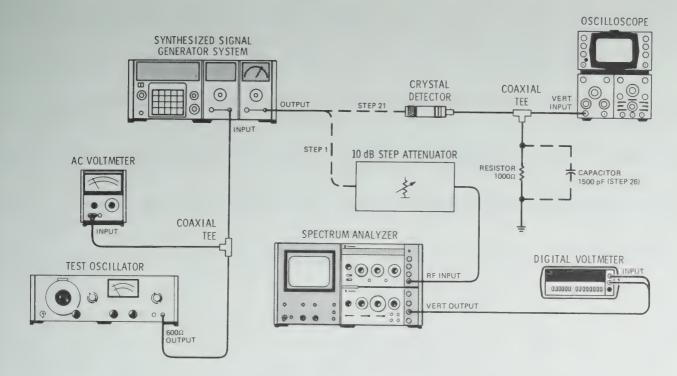


Figure 4-6. Amplitude Modulation Depth and 3 dB Bandwidth Test Setup

EQUIPMENT:

Test Oscillator	۰								۰	HP 651B
AC Voltmeter					٠	٠		٠		HP 403B
10 dB Step Attenuator										
Spectrum Analyzer	۰		۰	۰	٠				٠	HP 8555A/8552B/140T
Digital Voltmeter			٠			٠	٠	٠	٠	HP 3466A
Coaxial Tee (2 required)										HP 1250-0781
Crystal Detector		٠	٠	٠				٠		HP 423A
Oscilloscope				٠	۰			٠	٠	HP 180C/1801A/1821A
Resistor 1 K										HP 0757-0280

- 1. Connect the equipment as shown in Figure 4-6 (step 1).
- 2. Set the synthesized signal generator controls as follows: center frequency 30 MHz, OUTPUT RANGE —10 dBm, VERNIER control for a panel meter reading of 0 dB, and AM off.
- 3. Let the spectrum analyzer warm up for 1 hour to minimize drift of the spectrum analyzer detector output. Set 10 dB step attenuator to 10 dB attenuation.
- 4. Set the spectrum analyzer center frequency to 30 MHz, frequency span per division 5 MHz, resolution bandwidth 300 kHz; input attenuation to 20 dB, and vertical sensitivity per division 10 dB. Adjust the center frequency control to center the display. Set the frequency span to zero and tune to peak the trace.

4-18. AMPLITUDE MODULATION DEPTH AND 3 dB BANDWIDTH (Cont'd)

NOTE

Throughout this test, continually check that the signal is peaked for maximum deflection. Tune the center frequency control for maximum signal deflection.

5.	Set the vertical scale	to linear ar	nd adjust	the reference	level v	vernier	for a o	digital	voltmeter	reading	of
	-200 mVdc.										

6. Set the 10 dB step attenuator to 0 dB and record the digital voltmeter reading.

____mVdc

7. Set the 10 dB Step Attenuator to 20 dB and record the digital voltmeter reading.

_____mVdc

8. Calculate the offset voltage using the following formula:

$$V_{off} = \frac{mVdc + 200\alpha}{1-\alpha}$$

where

 $V_{\rm off}$ is the offset voltage in millivolts mVdc is the DVM reading in millivolts α is 3.16 (step 6) or 0.316 (step 7).

For example:

$$mVdc = -687$$
 in step 6.

therefore
$$V_{off} = \frac{-687 + 200 (3.16)}{1 - (3.16)} = +25.5 \text{ mVdc}$$

- 9. Find the value of $V_{\rm off}$ for step 7. The difference between the two should be <4 mVdc. Use the average value of $V_{\rm off}$.
- 10. Set the 10 dB step attenuator to 10 dB.
- 11. Set the system center frequency to 500 MHz, the modulation mode to AM, the modulation source to external, and a modulation level of 30% (0.3 Vrms input to an Auxiliary Section; 1.5 Vrms to a Modulation Section) at a 1 kHz rate.
- 12. Set the spectrum analyzer center frequency control to 500 MHz, frequency span to zero, and peak the trace. Set the reference level vernier for a digital voltmeter reading of -283 mVdc + V_{off}. See Steps 8 and 9.
- 13. Set the DVM controls to measure the peak detector's ac component. The modulation level (%) is 1/2 (one-half) the DVM reading (Vrms). Record the reading for 30% AM.

50 mVrms_____70 mVrms

14. Set the modulation section (test oscillator) controls for 70% AM. Record the DVM reading.

130 mVrms 150 mVrms

Model 86603A Performance Tests

PERFORMANCE TESTS

	FENTONIMANCE 1E313
4-18	. AMPLITUDE MODULATION DEPTH AND 3 dB BANDWIDTH (Cont'd)
15.	Set the modulation section (test oscillator) controls for 90% AM. Record the DVM reading 170 mVrms190 mVrms
16.	Set the system center frequency to 1500 MHz; set the modulation mode switch to OFF.
17.	Set the spectrum analyzer controls to display the 1500 MHz signal. Set the frequency span to zero. Adjust the center frequency control to peak the trace.
18.	Set the system modulation mode to AM, an external source, and a modulation level of 50% (0.5 Vrms input to an auxiliary section; 1.5 Vrms to a modulation section) at a 1 kHz rate.
19.	Set the spectrum analyzer's reference level to give a digital voltmeter reading of $-283~\rm mVdc$ + $V_{\rm off}$. See Steps 8 and 9.
20.	Set the DVM controls to measure the ac component of the peak detector output. Record the reading for 50% AM.
	80 mVrms120 mVrms
21.	Connect the crystal detector to the RF Section OUTPUT jack.
22.	Set the modulation section and test oscillator controls for an AM level of 30% (0.3 Vrms input to an auxiliary section; 1.5 Vrms to a modulation section) at a 1 kHz rate.
2 3.	Set the oscilloscope controls for a 5 division peak-to-peak display of the demodulated signal.
24.	Increase the test oscillator frequency to 5 kHz. The signal amplitude should be \geq 3.5 divisions peakto-peak.
	3.5 div p-p
25.	Repeat steps 22 through 24 with center frequency set to 500 MHz. Increase the test oscillator frequency from 5 to 100 kHz. Record the signal amplitude.
	3.5 div p-p
26.	Install the 1500 pF capacitor as shown in Figure 4-6.
27.	Repeat steps 22 through 24 with center frequency set to 9 MHz. Increase the test oscillator frequency from 5 to 10 kHz. Record the signal amplitude.
	3.5 div p-p

4-19. FREQUENCY MODULATION RATE AND DEVIATION

SPECIFICATION:

Rate: DC to 200 kHz with the 86632B or the 86635A: 20 Hz to 100 kHz with the 86633B.

4-19. FREQUENCY MODULATION RATE AND DEVIATION (Cont'd)

Maximum Deviation (Peak):

At center frequencies <1300 MHz, 200 kHz with the 86632B or the 86635A; 100 kHz with the 86633B At center frequencies >1300 MHz, 200 kHz with the 86632B or the 86635A, 200 kHz with the 86633B.

NOTE

To check the frequency modulation rate and deviation, refer to the performance test in Section IV of the applicable modulation section manual.

4-20. OUTPUT IMPEDANCE TEST

SPECIFICATION:

Impedance: 50Ω

VSWR: <2.0 on +10 and 0 dBm ranges; <1.3 on -10 dBm range and below.

DESCRIPTION:

The Synthesized Signal Generator System's output signal is reflected back into the RF OUTPUT jack by a coaxial short at the end of an adjustable stub (a variable length of air-line). This reflected signal is rereflected by any mismatch at the jack. The re-reflected signal combines with the output signal according to the relative phase and magnitude of the two signals. The combined signal is monitored by a directional coupler and then measured by a voltmeter or spectrum analyzer. Maximum and minimum power levels are noted as the electrical length of the stub is varied (i.e., the electrical distance from the RF OUTPUT jack to the coaxial short is varied). The maximum allowable change in voltage or dB is calculated from the following formulas.

$$VSWR = \frac{V_{max}}{V_{min}}$$

$$dB = 20 \log \left(\frac{V_{max}}{V_{min}}\right)$$

$$dB = 20 \log (VSWR)$$

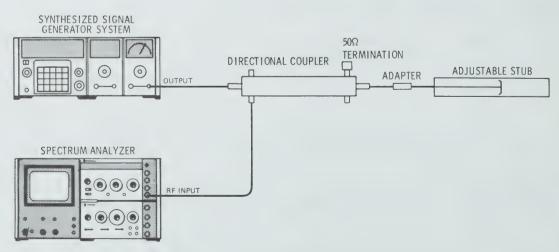


Figure 4-7. Output Impedance Test Setup

4-20. OUTPUT IMPEDANCE TEST (Cont'd)

EQUIPMENT:

Adapter (Male Type N to GR 874) HP 1250-0847

Adjustable Stub General Radio 874-D50L Spectrum Analyzer HP 8555A/8552B/140T

 50Ω Termination HP 11593A

PROCEDURE:

- Set the Synthesized Signal Generator system center frequency to 500 MHz, the OUTPUT RANGE switch to +10 dBm, and the VERNIER control for a panel meter reading of 0 dB.
- 2. Set up the equipment as shown in Figure 4-7.
- Set the spectrum analyzer controls for a convenient display of the signal. Set the vertical sensitivity 3. to 2 dB per division
- Adjust the stub for a minimum indication on the spectrum analyzer display. Adjust the reference level range and vernier controls for a convenient reference level.
- 5. Adjust the stub for a maximum indication on the display. The signal level increase should be <6 dB (VSWR < 2.0).

6 dB

- Set the system's OUTPUT RANGE switch to 0 dBm. Adjust the VERNIER control for a panel meter 6. reading of +3 dB.
- 7. Repeat steps 3 and 4. The signal level increase should be <6 dB (VSWR <2.0).

_6 dB

- Set the system's OUTPUT RANGE switch to -10 dBm. 8.
- 9. Repeat steps 3 and 4. The signal level increase should be <2.3 dB (VSWR <1.3).

2.3 dB

10. If desired, repeat at other frequencies between 100 MHz and 2 GHz.

NOTE

The steps given above effectively check VSWR at all settings of the output attenuator.

4-21. SIGNAL-TO-PHASE NOISE RATIO

SPECIFICATION:

In the CW, AM, and ϕ M modes, greater than 45 dB in a 30 kHz band centered on the carrier and excluding a 1 Hz band centered on the carrier at center frequencies <1300 MHz; >39 dB in a 30 kHz band centered on the signal excluding a 1 Hz band centered on the carrier at center frequencies ≥1300 MHz.

4-21. SIGNAL-TO-PHASE NOISE RATIO (Cont'd)

DESCRIPTION:

AC voltage measurements proportional to carrier amplitude and residual carrier phase deviation are compared for the signal-to-phase noise ratio. The Synthesized Signal Generator System's reference and RF OUTPUT (carrier) signals are mixed and the difference frequency is monitored by an oscilloscope and ac voltmeter. The mixer output (proportional to the carrier amplitude) is noted. The two signals are then frequency synchronized with phase difference of 180° . (This phase difference provides maximum resolution for voltage measurements at the mixer output which are proportional to the change of phase of the RF OUTPUT signal.) This ac voltage is proportional to the phase noise and when compared to the carrier voltage yields the signal-to-phase noise ratio.

NOTE

A 3 dB correction factor takes into account the non-correlated noise contribution of the reference system. The noise levels of the reference system and system under test are assumed to be equal.

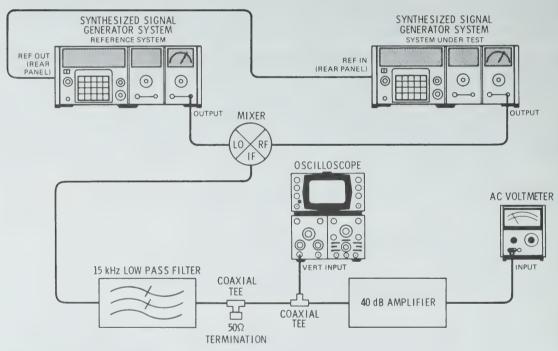


Figure 4-8. Signal-to-Phase Noise Ratio Test Setup

EQUIPMENT:

Synthesized Signal Generator System	٠	٠			HP 8660C/86603A/86631B
Oscilloscope			a		HP 180C/1801A/1821A
Coaxial Tee	٠			۰	HP 1250-0781 (BNC)
Double Balanced Mixer					Watkins-Johnson M1J
AC Voltmeter	٠				HP 403B
40 dB Amplifier	٠				HP 08640-60506
15 kHz Low Pass Filter					
50Ω Termination					HP 11593A

4-21. SIGNAL-TO-PHASE NOISE RATIO (Cont'd)

PROCEDURE:

- 1. Set the controls of the system under test as follows: center frequency 500.001000 MHz and the output level to -47 dBm (OUTPUT RANGE switch set to -50 dBm).
- 2. Set the controls of the reference system as follows: center frequency 500.000000 MHz and the output level to +7 dBm.
- 3. Connect the equipment as shown in Figure 4-8.
- 4. Record the relative ac voltmeter reading.

_____dB

- 5. Set the system under test OUTPUT RANGE switch to -10 dBm (-7 dBm output level).
- 6. Adjust the oscilloscope display of the 1 kHz signal for an amplitude of eight divisions. Set the oscilloscope vertical input to ground and adjust the vertical position control so the trace lies over the center horizontal line of the graticule. Set the vertical input to dc coupled.
- 7. Set the system under test center frequency to 500.000001 MHz and note that oscilloscope baseline trace alternately rises and falls over eight-division display. (500.0001 MHz; Option 004).
- 8. Reset the center frequency to 500.000000 MHz at a time that causes the oscilloscope baseline trace to stop within $\pm 1/10$ division of the center horizontal line of the graticule.
- 9. Read the noise level on the ac voltmeter. Signal-to-phase noise ratio equals the sum of the attenuator change and the reference system noise contribution minus the change in the voltmeter reading. Signal-to-phase noise ratio = $40 \text{ dB} + 3 \text{ dB} (\pm \Delta \text{ dB})$. For example, the voltmeter reading is 8 dB below the reference (-8 dB). Therefore, the Signal-to-phase noise ratio = 40 + 3 (-8) = 51 dB down. Record the ratio.

45 dB down

- 10. Set the controls of the system under test as follows: center frequency 1500.001000 MHz and the output level to -37 dBm (OUTPUT RANGE -40 dBm).
- 11. Set the controls of the reference system as follows: center frequency 1500.000000 MHz and the output level to +7 dBm.
- 12. Record relative AC voltmeter reading.

dB

- 13. Set the system under test OUTPUT RANGE switch to -10 dBm. (-7 dBm output level).
- 14. Adjust the oscilloscope display of the 1 kHz signal for an amplitude of eight divisions. Set the oscilloscope vertical input to ground and adjust the vertical position control so the trace lies over the center horizontal line of the graticule. Set the vertical input to dc coupled.
- 15. Set the system under test center frequency to 1500.000002 MHz and note that oscilloscope baseline trace alternately rises and falls over eight-division display. (1500.0002 MHz; Option 004).

4-21. SIGNAL-TO-PHASE NOISE RATIO (Cont'd)

- 16. Reset the center frequency to 1500.000000 MHz at a time that causes the oscilloscope baseline trace to stop within $\pm 1/10$ division of the center horizontal line of the graticule.
- 17. Read the noise level on the ac voltmeter. Signal-to-phase noise ratio = 33 dB $-(\pm \Delta dB)$.

39 dB down_____

4-22. SIGNAL-TO-AM NOISE RATIO

SPECIFICATION:

Greater than 65 dB in a 30 kHz bandwidth centered on the carrier excluding a 1 Hz band centered on the carrier.

DESCRIPTION:

A comparison of voltage measurements proportional to carrier amplitude and AM noise yields the signal-to-AM noise ratio. First, a carrier reference level is determined by measuring the detected AC voltage for 30% AM (the detected signal is 10.5 dB below the carrier level). Then the AM noise level is measured and the signal-to-AM noise ratio is determined.

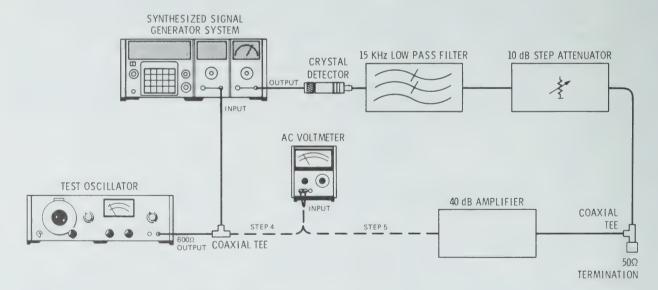


Figure 4-9. Signal-to-AM Noise Ratio Test Setup.

EQUIPMENT:

10 dB Step Attenuator						۰			٠		HP 355D Option H38
40 dB Amplifier		٠									HP 08640-60506
15 kHz Low Pass Filter		٠		٠				٠	٠	٠	HP 86602-60054
Crystal Detector		٠			٠				٠		HP 423A
Test Oscillator											
50Ω Termination							٠				HP 11593A
Coaxial Tee (2 required)			a	٠		٠				٠	HP 1250-0781
AC Voltmeter	٠			4							HP 403B

4-22. SIGNAL-TO-AM NOISE RATIO (Cont'd)

PROCEDURE:

- 1. Set the 10 dB step attenuator to 50 dB.
- 2. Set the system center frequency to 500 MHz and the RF output level to +3 dBm (0 dBm OUTPUT RANGE).
- 3. Connect the equipment as shown in Figure 4-9.
- 4. Set the system's modulation section controls for the AM mode and an external modulation source. The modulation level control and/or the test oscillator controls are set for a modulation level of 30% (0.3 Vrms to an auxiliary section; 1.5 Vrms to a modulation section) at a 1 kHz rate.

NOTE

The ac voltmeter can be used to monitor the modulation or auxiliary section input voltage while it is being set.

ວ.	Record the ac voltmeter reading of the 40 dB amplifier output in dB.
	dB
6.	Set the system's modulation mode to off.
7.	Set the 10 dB step attenuator to 0 dB.
8.	Record the ac voltmeter reading.
	dB
9.	The signal-to-AM noise ratio is equal to the sum of the change in attenuation level and the level of the 30% AM level relative to the carrier minus the change in ac voltmeter reading in dB. Therefore, signal-to-AM noise ratio = $50 \text{ dB} + 10.5 \text{ dB} - (\pm \Delta \text{ dB})$. For example, the ac voltmeter reading is 12 dB down (below) the reference level and the signal-to-AM noise ratio = $50 + 10.5 - (-12)$ or 72.5 dB down.
10.	Record the ratio.
	65 dB down
11.	Repeat the entire procedure using a system center frequency of 2 GHz. Record, the signal-to-AM noise ratio.
	65 dB down
4-23	RESIDUAL FM

SPECIFICATION:

In the FM X0.1 Mode, <10 Hz-rms average in a 300 Hz to 3 kHz post-detection band at center frequencies <1300 MHz; <20 Hz-rms average at center frequencies >1300 MHz.

4-23. RESIDUAL FM (Cont'd)

DESCRIPTION:

The RF output of the synthesized signal generator in FM mode with no modulating signal applied is measured with a modulation analyzer and residual FM is read directly.

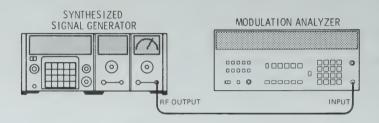


Figure 4-10. Residual FM Test Setup

EQUIPMENT:

Modulation Analyzer HP 8901A

PROCEDURE:

- 1. Set the synthesized signal generator to 1200.0 MHz, output level to +10 dBm, modulation mode to FM x 0.1, and modulation source to external ac (leveled). There should be no input to the modulation section front panel connector. Turn the modulation level control full clockwise.
- 2. Measure FM using the modulation analyzer with 300 Hz high pass and 3 kHz low pass filters enabled. Reading (avg.) should be less than 10 Hz.

4-24. AMPLITUDE MODULATION DISTORTION

SPECIFICATION:

For center frequencies <1300 MHz, AM distortion at 30% AM is <1%, at 70% AM is <3%, and at 90% AM is <5%. For center frequencies ≥ 1300 MHz, AM distortion at 30% is <5%.

NOTES

- 1. The AM distortion specification applies only at 400 and 1000 Hz rates, with a front panel meter indication of 0 to +3 dB, and at OUTPUT RANGE switch settings of \leq 0 dBm. At a meter indication of -6 dB, the distortion approximately doubles. The modulating signal distortion must be <0.3% for the system performance to meet the specifications.
- 2. If the signal generator system does not meet the AM distortion specification, refer to the Systems Trouble-shooting information in Section VIII (Service Sheet 1) in this manual.

4-24. AMPLITUDE MODULATION DISTORTION (Cont'd)

DESCRIPTION:

The output of the synthesized signal generator is amplitude modulated. A modulation analyzer demodulates the output signal and distortion of the demodulated signal is measured.

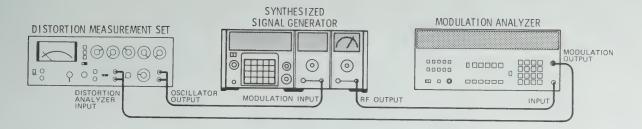


Figure 4-11. Amplitude Modulation Distortion Test Setup

EQUIPMENT:

- 1. Connect the equipment as shown in Figure 4-11.
- 2. Set the synthesized signal generator center frequency to 1000.0 MHz, output level to -20 dBm and modulation mode to AM with external ac coupled source.
- 3. Set the distortion measurement set to 1000 Hz. If an 86632 or 86633 modulation section is being used, set the oscillator output level to 1.5 Vrms and adjust the modulation section level control to give a 30% reading on the meter. If an 86631 modulation section is being used, set the oscillator output level to 0.3 Vrms.
- 4. Set the modulation analyzer to AM mode. Use 50 Hz high pass and 15 kHz low pass post detection filters. Measure distortion of the modulation output signal. Distortion should be less than 1%.
- 5. Repeat the distortion measurement at AM modulation depths of 70% and 90% (oscillator output levels of 0.70 Vrms and 0.90 Vrms into an 86631). Distortion should be less than 3% and 5%, respectively.

4-25. INCIDENTAL PHASE MODULATION

SPECIFICATION:

At 30% AM <0.2 radians at center frequencies <1300 MHz, <0.4 radians at center frequencies ≥1300 MHz.

DESCRIPTION:

The synthesized signal generator is amplitude modulated and incidental phase modulation is measured directly on the modulation analyzer.

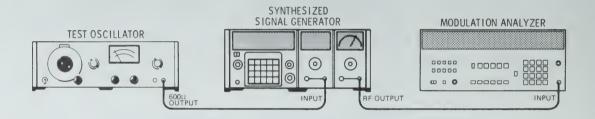


Figure 4-12. Incidental Phase Modulation Test Setup

EQUIPMENT:

- 1. Connect the equipment as shown in Figure 4-12.
- 2. Set the synthesized signal generator to 500 MHz center frequency and -10 dBm output level.
- 3. Set the test oscillator frequency to 1000 Hz. If an 86632 or 86633 modulation section is used, set the test oscillator output level to 1.5 Vrms. Set the modulation mode to AM and modulation source to external dc. Adjust the modulation level control for a meter reading of 30%. If an 86631 auxiliary section is being used, set the test oscillator output level to 0.30 Vrms.
- 4. Measure phase modulation on the modulation analyzer with the 50 Hz high pass and 15 kHz low pass filters enabled. The reading should be less than 0.2 radians.

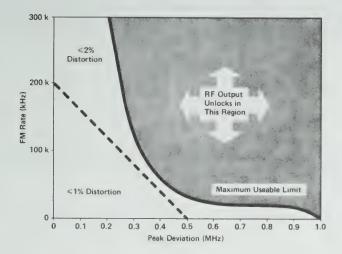
4-26. FREQUENCY MODULATION DISTORTION

SPECIFICATION:

Total harmonic distortion for modulation rates up to 20 kHz, <1% up to 200 kHz peak deviation for center frequencies <1300 MHz; <1% up to 400 kHz peak deviation for center frequencies >1300 MHz. Distortion from an external source must be <0.3% to meet these specifications.

NOTES

- 1. In the FM mode, typical Residual FM in a 0.3 to 3 kHz audio bandwidth is <15 Hz and may limit minimum Noise and Distortion measurement at deviations <2 kHz peak.
- 2. If the signal generator system does not meet the FM distortion specification, refer to the System's Trouble-shooting information in Section VIII (Service Sheet 1) in this manual.



Typical FM Distortion Curve

DESCRIPTION:

The output of the synthesized signal generator is phase modulated. A modulation analyzer demodulates the signal generator output signal and distortion of the demodulated signal is measured.

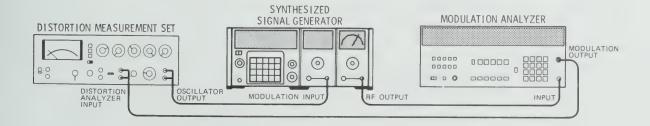


Figure 4-13. Frequency Modulation Test Setup

4-26. FREQUENCY MODULATION DISTORTION (Cont'd)

EQUIPMENT:

PROCEDURE:

- 1. Connect equipment as shown in Figure 4-13.
- 2. Set the synthesized signal generator center frequency to 500.0 MHz, output level to +7 dBm, modulation mode to FM x 10 (FM x 1 on 86633) and modulation source to external ac coupled.
- 3. Set the distortion measurement set to 10 kHz frequency and audio oscillator output level to 1.50 Vrms.
- 4. Adjust the modulation level control on the signal generator to give a modulation section meter reading of 200 kHz (100 kHz with a 86633 modulation section).
- 5. Set the modulation analyzer to FM mode. Use 50 Hz high pass and no low pass post-detection filters. Measure distortion of the modulation output signal. Distortion should be less than 1%.

4-27. INCIDENTAL AM

SPECIFICATION:

AM side bands >60 dB down from carrier with FM peak deviation of 75 kHz at a 1 kHz rate.

DESCRIPTION:

The synthesized signal generator is frequency modulated and incidental AM is measured directly by the modulation analyzer.

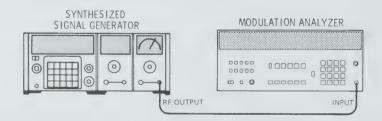


Figure 4-14. Incidental AM Test Setup

Performance Tests

PERFORMANCE TESTS

4-27. INCIDENTAL AM (Cont'd)

EQUIPMENT:

Modulation Analyzer HP 8901A

- 1. Connect the equipment as shown in Figure 4-14.
- 2. Set the synthesized signal generator to center frequency 100 MHz, output level +3 dBm, modulation mode FM x 1 and modulation source internal 1000. Adjust the modulation level control for a modulation section meter reading of 75 kHz.
- 3. Set the modulation analyzer to AM mode and enable the 50 Hz high pass and 15 kHz low pass filters. Reading should be less than 0.2%.

4-28. SPURIOUS SIGNALS, NARROWBAND

SPECIFICATION:

At center frequencies <1300 MHz all narrowband non-harmonically related spurious signals in the CW, AM, and ϕ M modes are:

80 dB down from carrier at frequencies < 700 MHz

80 dB down from carrier within 45 MHz of the carrier at frequencies ≥700 MHz

50 dB down from carrier on the +10 dBm range.

At center frequencies \geq 1300 MHz all narrowband non-harmonically related spurious signals in the CW, AM, and ϕ M modes are:

74 dB down from carrier within 45 MHz of the carrier for output levels ≤+3 dBm; slightly higher from +3 to +7 dBm.

ALL power line related spurious signals are 70 dB down from the carrier at center frequencies <1300 MHz; 64 dB down from the carrier at center frequencies ≥1300 MHz.

DESCRIPTION:

The outputs of two Synthesized Signal Generator Systems which use the same time base reference are mixed and the difference frequency is amplified and coupled to the wave analyzer. A reference level is established, various selected frequencies are then set on the two generator systems, and the spurious signal levels are measured.

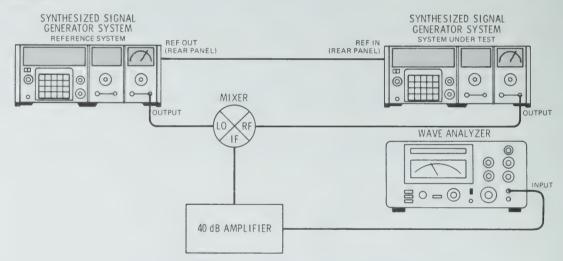


Figure 4-15. Narrowband Spurious Signal Test Setup

EQUIPMENT:

- 1. Connect the equipment as illustrated in Figure 4-15.
- 2. Connect the rear panel Reference Output (Reference System) to System Under Test rear panel Reference Input. Set the Reference Selector switch of the systems to internal and external respectively.
- 3. On reference system, set the center frequency to 500.001 MHz, the OUTPUT RANGE switch to +10 dBm, and adjust VERNIER control to a -3 dB meter reading.

Model 86603A Performance Tests

PERFORMANCE TESTS

4-28. SPURIOUS SIGNALS, NARROWBAND (Cont'd)

- 4. On system under test, set mainframe center frequency to 500 MHz, Model 86603A OUTPUT RANGE switch to -80 dBm, and adjust VERNIER control to 0 dB indication on meter scale.
- 5. Set wave analyzer scale switch to 90 dB, amplitude reference to -60, dBv mode, resolution bandwidth 3 Hz, display smoothing to max, and AFC to on.
- 6. Set wave analyzer frequency control to 1 kHz and adjust the input sensitivity for a 0 dB indication on meter scale.
- 7. On system under test, set the OUTPUT RANGE switch to -10 dBm and adjust VERNIER to 0 dB indication on meter scale.
- 8. On reference system and system under test, set mainframe center frequency values to those listed in Table 4-2 below 1300 MHz and verify that levels of corresponding spurious signals are in accordance with specification. The corrected reading of spurious level relative to carrier is 70 dB (± difference level), therefore a reading of —13 dB relative to the reference level (step 6) gives the spurious signal . level. 70 dB (—13 dB) = 83 dB down.

NOTE

It may be necessary to slightly readjust the Wave Analyzer Frequency control to locate the spurious signal.

System Under Test	Reference System	Level Measured (dB down)
100.280000 MHz	100.561000 MHz	80 dB
200.280000 MHz	200.561000 MHz	80 dB
409.720000 MHz	409.441000 MHz	80 dB
509.720000 MHz	509.441000 MHz	80 dB
1109.720000 MHz	1109.441000 MHz	80 dB
1209.720000 MHz	1209.441000 MHz	80 dB
2400.000000 MHz	2400.101000 MHz	74 dB
2400.000000 MHz	2400.201000 MHz	74 dB
2400.000000 MHz	2400.301000 MHz	74 dB
2400.000000 MHz	2400.401000 MHz	74 dB

Table 4-1. Narrowband Spurious Signals Checks

- 9. Repeat steps 3 and 7 with a reference system center frequency of 2400.001 MHz and a System Under Test center frequency of 2400 MHz.
- 10. Repeat step 8 using the center frequencies ≥ 1300 MHz as shown in Table 4-2.

4-29. SPURIOUS SIGNALS, WIDEBAND

SPECIFICATION:

At center frequencies <1300 MHz, all wideband non-harmonically related spurious signals in the CW, AM, and ϕ M modes are:

80 dB down from carrier at frequencies < 700 MHz

70 dB down from carrier >45 MHz from carrier at frequencies ≥700 MHz

50 dB down from carrier on the +10 dBm range.

At center frequencies \geq 1300 MHz all wideband non-harmonically related spurious signals in the CW, AM, and ϕ M modes are:

64 dB down from carrier >45 MHz from carrier for output levels ≤+3 dBm; slightly higher from +3 to +7 dBm.

DESCRIPTION:

The RF OUTPUT of the Synthesized Signal Generator System is monitored by a spectrum analyzer after being passed through a 2200 MHz lowpass filter. Selected signals which fall within the specified range are measured.

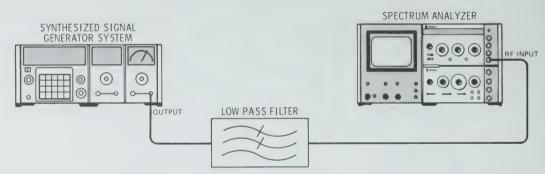


Figure 4-16. Wideband Spurious Signal Test Setup

EQUIPMENT:

- 1. Connect equipment as illustrated in Figure 4-16.
- 2. With Model 86603A OUTPUT RANGE switch set to +10 dBm and VERNIER control adjusted for 0 dB meter indication, set mainframe center frequency to those values listed in Table 4-3 below 1300 MHz and adjust the Spectrum Analyzer to measure corresponding spurious signal level relative to the carrier.
- 3. Remove the low pass filter and set the RF Section output level to +3 dBm (0 dBm range).
- 4. Set the System Center Frequency to those values listed in Table 4-3 above 1300 MHz. Adjust the spectrum analyzer controls to measure the spurious signals relative to the carrier.

Model 86603A Performance Tests

PERFORMANCE TESTS

4-29. SPURIOUS SIGNALS, WIDEBAND (Cont'd)

Table 4-2. Wideband Spurious Signals Checks

Mainframe Frequency	Spurious Frequency	Level Measured
1299.9 MHz	150 MHz 1150 MHz 1450 MHz	50 dB down 50 dB down 50 dB down
1000 MHz	950 MHz 1050 MHz	50 dB down 50 dB down
999.9 MHz	950 MHz 1050 MHz	50 dB down 50 dB down
800.0 MHz 799.9 MHz	750 MHz 850 MHz	50 dB down 50 dB down
2000 MHz	1950 MHz 2050 MHz	64 dB down
1999.9 MHz	1950 MHz 2050 MHz	64 dB down 64 dB down

4-30. PHASE MODULATION PEAK DEVIATION TEST

SPECIFICATION:

0 to 100 degrees peak at center frequencies <1300 MHz. May be overdriven to 2 radians (115°) in Modulation Section external dc mode. 0 to 200 degrees peak at center frequencies \ge 1300 MHz. May be overdriven to 2 radians (230°) in Modulation Section external dc mode.

NOTE

To check Phase Modulation peak deviation, refer to Section IV of the appropriate Modulation Section Operating and Service Manual.

4-31A. PHASE MODULATION DISTORTION

SPECIFICATION:

<5% up to 1 MHz rates

<7% up to 5 MHz rates

<15% up to 10 MHz rates

Modulation distortion from an external source must be less than 0.3% to meet these specifications.

4-31A, PHASE MODULATION DISTORTION (Cont'd)

NOTES

- 1. Using this procedure, the proof of performance for phase modulation distortion is valid only when the HP Model 86635A Modulation Section is being used in the signal generator system. The change in distortion level from the 20 Hz rate, as used in this procedure, to the maximum 1 MHz rate is minimal. This procedure is, however, not a complete check for the Model 86634A which can use modulation rates up to 10 MHz.
- 2. If the signal generator system does not meet the ϕM distortion specification, refer to the Systems Troubleshooting information in Section VIII (Service Sheet 1) in this manual.

DESCRIPTION:

The output of the synthesized signal generator is frequency modulated. A modulation analyzer demodulates the signal generator output signal and distortion of the demodulated signal is measured.

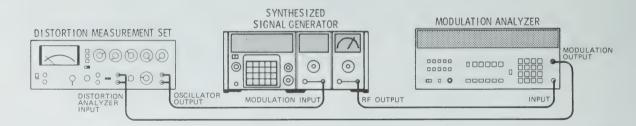


Figure 4-17A. Phase Modulation Distortion Test Setup

EQUIPMENT:

- 1. Connect equipment as shown in Figure 4-17A
- 2. Set the synthesized signal generator center frequency to 10.0 MHz, output level to +3 dBm, modulation mode to Φ M, and modulation source to external ac.
- 3. Set the distortion measurement set to 200 Hz and audio oscillator output level to 1.50 Vrms.
- 4. Adjust the modulation level control on the signal generator to give a modulation section meter reading of 100° .
- 5. Set the modulation analyzer to Φ M mode. Use 50 Hz high pass and 15 kHz low pass post detection filters. Measure distortion of the modulation output signal. Distortion should be less than 5%.

Model 86603A Performance Tests

PERFORMANCE TESTS

4-31B. PHASE MODULATION DISTORTION - ALTERNATE PROCEDURE

SPECIFICATION:

<5% up to 1 MHz rates

<7% up to 5 MHz rates

<15% up to 10 MHz rates

NOTES

- 1. The HP Model 86635A Modulation Section has a maximum specified phase modulation rate of 1 MHz. Therefore, only the <5% distortion specification is applicable. Because the maximum modulation rate of the Model 86634A is 10 MHz, all the specified distortion levels apply.
- 2. If the signal generator system does not meet the ϕM distortion specification, refer to the Systems Troubleshooting information in Section VIII (Service Sheet 1) in this manual.

DESCRIPTION:

The phase modulated output of the System Under Test is demodulated using a phase modulation test set. The harmonic levels are measured with a spectrum analyzer and the total harmonic distortion is calculated. A low pass filter is used between test oscillator and modulation section to insure that the modulation drive signal has less than 0.3% distortion.

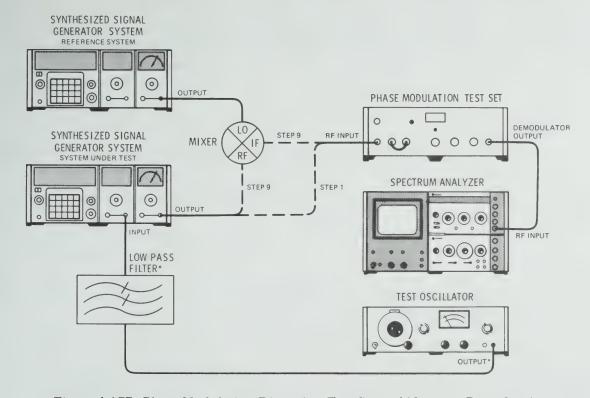


Figure 4-17B. Phase Modulation Distortion Test Setup (Alternate Procedure)

^{*}In Figure 4-17B the test oscillator output impedance and Low Pass Filter impedance is 50 ohms when the modulation section is a Model 86634A and 600 ohms with a Model 86635A.

4-31B. PHASE MODULATION DISTORTION - ALTERNATE PROCEDURE (Cont'd)

EQUIPMENT:

PROCEDURE:

- 1. Set the Test Oscillator to 1 MHz, connect a 1 MHz low pass filter (50 ohm for 86634A, 600 ohm for 86635A) to appropriate test oscillator output and adjust for 1.7 Vrms output. Connect the rest of the equipment as shown in Figure 4-17B.
- 2. Set the system under test for 300 MHz center frequency and +3 dBm output (0 dBm range). Connect the RF output jack directly to the RF input of the phase modulation test set.
- 3. Set the system under test controls for ϕM with a modulation level of 100° peak deviation.
- 4. View the signal generator output on the spectrum analyzer display. Record the level of the second and third harmonics of the demodulated output signal with respect to the fundamental.
- 5. Use Table 4-1 to obtain power ratios of the harmonics. Then use Table 4-1 to find the dB level corresponding to sum of the two ratios. The resultant level should be <5% or ≥ 26 dB down.

86634A 26 dB down _____

- 6. Set the center frequency of the system under test to 299.9 MHz.
- 7. Set the test oscillator to 1 MHz (10 MHz), connect the 1 MHz (10 MHz) low pass filter to the appropriate oscillator output (50 or 600Ω) and adjust for an output of 1.7 Vrms.
- 8. Repeat steps 3, 4 and 5. Total harmonic distortion should be <5% or ≥ 26 dB down (<15% or ≥ 16.5 dB down).

86634A 16.5 dB down _____ 86635A 26 dB down _____

- 9. Set the center frequency of the system under test to 1900 MHz. Connect the mixer and the reference system as shown in Figure 4-16B.
- 10. Set the reference system center frequency to 1600 MHz with an RF output level of +7 dBm.
- 11. Increase the RF output level of the system under test (if necessary) until the phase modulation test set phase locks.

PERFORMANCE TESTS

4-31B. PHASE MODULATION DISTORTION - ALTERNATE PROCEDURE (Cont'd)

- 12. Set the test oscillator frequency to 1 MHz (5 MHz). Connect the 1 MHz (5 MHz) low pass filter (50 or 600Ω) to the oscillator output. Adjust the test oscillator output level to 1.7 Vrms. Set the system under test modulation level to 200° peak deviation.

Table 4-3. Performance Test Record (1 of 7)

Mode RF S	els 86603A/11661 Section/Frequency Extension Module	ested Byate							
- Seria	D.								
Para.	Took	Results							
No.	Test	Min.	Actual	Max.					
4-9.	FREQUENCY RANGE								
	Step 3 1.000 000 MHz Step 4 1299.999 999 MHz Step 5 2599.999 998 MHz	-1 Hz -1 Hz -1 Hz		+1 Hz +1 Hz +1 Hz					
4-11.	FREQUENCY SWITCHING TIME 6 ms to be within 50 Hz of any new frequency Step 9 30.000 000 MHz ±50 Hz Step 10 29.999 999 MHz ±50 Hz	-50 Hz -50 Hz		+50 Hz +50 Hz					
	100 ms to be within 5 Hz of any new frequency Step 14	-5 Hz -5 Hz		+5 Hz +5 Hz					
4-12.	OUTPUT LEVEL SWITCHING TIME								
	Remote programming of level change on same range accomplished in 5 ms, maximum, at 50 MHz								
	Step 4 10 to 19 dB			5 ms					
	Level change to another range accomplished in 50 ms, maximum, at 50 MHz.								
	Step 5 10 to 30 dB			50 ms					
	Remote programming of level change on same range accomplished in 5 ms, maximum, at 1 MHz								
	Step 6 10 to 19 dB			5 ms					
	Remote programming of level change on same range accomplished in 5 ms, maximum, at 2599 MHz.								
	Step 7 10 to 19 dB			5 ms					

Model 86603A Performance Tests

Table 4-3. Performance Test Record (2 of 7)

Para.	-	Results				
No.	Test		Min.	Actual	Max.	
4-13A.	OUTPUT ACCURACY OUTPUT RANGE Front Pan	nel Meter Reading				
	+10 dBm*	0 dB	+7.5 dBm		+12.5 dBr	
		-3 dB	+4.5 dBm		+9.5 dBm	
		-6 dB	+1.5 dBm		+6.5 dBm	
	1	-6 dB	-8.5 dBm		-3.5 dBm	
	0 dBm	−3 dB	-5.5 dBm		-0.5 dBm	
	0 dBm	0 dB	-2.5 dBm		+2.5 dBm	
	0 dBm	+3 dB	+0.5 dBm		+5.5 dBm	
	—10 dBm	+3 dB	-9.5 dBm		-4.5 dBm	
		+3 dB	-19.5 dBm		-14.5 dBi	
	—30 dBm	+3 dB	-29.5 dBm		-24.5 dBi	
	—40 dBm	+3 dB	-39.5 dBm		-34.5 dBr	
	—50 dBm	+3 dB	-49.5 dBm		-44.5 dBr	
	I .	+3 dB	-59.5 dBm		-54.5 dBr	
		+3 dB	─69.5 dBm		-64.5 dBr	
	1	+3 dB	-80.5 dBm		-73.5 dBi	
	l control of the cont	+3 dB	-90.5 dBm		-83.5 dBr	
		+3 dB	-100.5 dBm		-93.5 dBr	
		+3 dB	-110.5 dBm		-103.5 dE	
		+3 dB	-120.5 dBm		-113.5 dI	
		+3 dB	-130.5 dBm		—123.5 dE	
4-13B.	OUTPUT ACCURACY – ALT	TERNATE				
	OUTPUT RANGE Front Pan	el Meter Reading				
	10 dBm*	0 dB	7.5 dBm		12.5 dE	
		-3 dB	4.5 dBm		9.5 dE	
		-6 dB	1.5 dBm		6.5 dE	
		−6 dB	-8.5 dBm		- 3.5 dE	
	0 dBm	-3 dB	-5.5 dBm		-0.5 dE	
	00 dBm	0 dB	-2.5 dBm		2.5 dE	
	0 dBm	3 dB	0.5 dBm		5.5 dE	
	-10 dBm	3 dB	-9.5 dBm		- 4.5 dE	
	-20 dBm	3 dB	-19.5 dBm		-14.5 dB	
	-30 dBm	3 dB	-29.5 dBm		-24.5 dE	
	-40 dBm	3 dB	-39.5 dBm		-34.5 dB	
	—50 dBm	3 dB	-49.5 dBm		-44.5 dB	
	-60 dBm	3 dB	-59.5 dBm		-54.5 dB	
	-70 dBm	3 dB	−69.5 dBm		-64.5 dB	
	-80 dBm	3 dB	-80.5 dBm		−73.5 dE	
	Level change from the -70 OUTPUT RANGE	to -80 dBm	9 dB		11 dB	

Table 4-3. Performance Test Record (3 of 7)

Para.	Test		Results		
No.	Test	Min.	Actual	Max.	
4-14.	OUTPUT FLATNESS				
	Reference level is -2.0 dBm at 1500 MHz.				
	1 MHz	-4.0 dBm		0.0 dBm	
	10 MHz	-4.0 dBm		0.0 dBm	
	100 MHz 500 MHz	-4.0 dBm -4.0 dBm		0.0 dBm 0.0 dBm	
	1000 MHz	-4.0 dBm		0.0 dBm	
	1299 MHz	-4.0 dBm		0.0 dBm	
	2000 MHz	-4.0 dBm		0.0 dBm	
	2599 MHz	-4.0 dBm		0.0 dBm	
4-15.	HARMONIC SIGNALS				
	OUTPUT RANGE = +10 dBm				
	Step 5 1299 MHz				
	Second Harmonic	25 dB down			
	Third Harmonic	25 dB down			
	Step 6 1000 MHz	05 10 1			
	Second Harmonic Third Harmonic	25 dB down 25 dB down			
	Step 6 500 MHz	20 db down			
	Second Harmonic	25 dB down			
	Third Harmonic	25 dB down			
	Step 6 100 MHz				
	Second Harmonic	25 dB down			
	Third Harmonic	25 dB down			
	Step 6 10 MHz	05 10 1			
	Second Harmonic Third Harmonic	25 dB down 25 dB down			
	OUTPUT RANGE = 0 dBm	20 db down			
	Step 7 100 MHz				
	Second Harmonic	30 dB down			
	Third Harmonic	30 dB down			
	Step 9 1400 MHz				
	Second Harmonic	20 dB down			
	Third Harmonic	20 dB down			
	Step 10 2500 MHz				
	Second Harmonic	20 dB down			
	Third Harmonic	20 dB down			
	Step 10 - Sub-Harmonics & Multiples				
	1400 MHz f/2	20 dB down			
	3f/2 2500 MHz f/2	20 dB down 20 dB down			
	3f/2	20 dB down			

Table 4-3. Performance Test Record (4 of 7)

Para.		Results				
No.	Test	Min.	Actual	Max.		
4-16.	PULSE MODULATION RISETIME Risetime (10% to 90% amplitude points)			50 ns		
4-17.	PULSE MODULATION ON/OFF RATIO Step 4 On/Off Ratio at <1300 MHz Step 5 On/Off Ratio at ≥1300 MHz	40 dB 60 dB				
4-18.	AMPLITUDE MODULATION DEPTH AND 3 dB BANDWIDTH Frequency = 500 MHz OUTPUT RANGE = -10 dBm Rate = 1 kHz Step 13 30% Step 14 70%	50 mVrms 130 mVrms		70 mVrms 150 mVrms		
	Step 15 90% Frequency = 1500 MHz	170 mVrms		190 mVrms		
	Step 20 Frequency = 1500 MHz OUTPUT RANGE = -10 dBm AM = 30% Step 24 1 kHz Rate (reference 5 div. p-p) AM less than 3 dB down	80 mVrms		120 mVrms		
	(>3.5 div. p-p) at 5 kHz Frequency = 500 MHz OUTPUT RANGE = -10 dBm AM = 30% Step 25 5 kHz rate (reference 5 div. p-p) AM less than 3 dB down	3.5 div. p-p				
	(>3.5 div. p-p) at 100 kHz Frequency = 9 MHz OUTPUT RANGE = -10 dBm AM = 30% Step 26 5 kHz rate (reference 5 div. p-p)	3.5 div. p-p				
	AM less than 3 dB down (>3.5 div. p-p)at 10 kHz	3.5 div. p-p				

Table 4-3. Performance Test Record (5 of 7)

Para.	Took	Results					
No.	Test	Min.	Actual	Max,			
4-20.	OUTPUT IMPEDANCE Center Frequency 500 MHz OUTPUT RANGE +10 dBm dB = 20 log (VSWR) dB = 6 for VSWR = 2.0			6 dB			
	OUTPUT RANGE 0 dBm dB = 6 for VSWR = 2.0			6 dB			
	OUTPUT RANGE —10 dBm dB = 2.3 for VSWR = 1.3			2.3 dB			
4-21.	SIGNAL-TO-PHASE NOISE RATIO Step 9 Noise Level Step 17 Noise Level	45 dB down 39 dB down					
4-22.	SIGNAL-TO-AM NOISE RATIO Step 10 Noise Level Step 11 Noise Level	65 dB down 65 dB down					
4-23.	RESIDUAL FM Center frequencies < 1300 MHz < 10 Hz-rms average						
4-24.	AMPLITUDE MODULATION DISTORTION Center frequencies <1300 MHz 30% AM						
	Total Distortion (<1%) 70% AM			1%			
	Total Distortion (<3%) 90% AM			3%			
	Total Distortion (<5%)			5%			
4-25.	INCIDENTAL PHASE MODULATION <0.2 radians-pk (11.5° pk)<1300 MHz			11.5°			
4-26.	FREQUENCY MODULATION DISTORTION Total Distortion <1%			1%			
4-27.	INCIDENTAL AM Incidental AM			0.2%			

Table 4-3. Performance Test Record (6 of 7)

ara. Test			Results				
Test		Min.	Actual	Max.			
Step 8 Spurious Respo	onse						
System Under Test	Reference Unit						
100.280000 MHz 200.280000 MHz 409.720000 MHz 509.720000 MHz 1109.720000 MHz 1209.720000 MHz 2400.000000 MHz 2400.000000 MHz 2400.000000 MHz 2400.000000 MHz	100.561000 MHz 200.561000 MHz 409.441000 MHz 509.441000 MHz 1109.441000 MHz 1209.441000 MHz 2400.101000 MHz 2400.201000 MHz 2400.301000 MHz 2400.401000 MHz	80 dB down 80 dB down 80 dB down 80 dB down 80 dB down 74 dB down 74 dB down 74 dB down 74 dB down					
(All spurious signals do 50 dB, minimum.)	own from carrier						
Mainframe Frequency 1299 MHz	Spur Frequency 150 MHz 1150 MHz 1450 MHz	50 dB down 50 dB down 50 dB down					
1000 MHz	950 MHz 1050 MHz	50 dB down 50 dB down					
999.9 MHz	950 MHz 1050 MHz	50 dB down 50 dB down					
800.0 MHz	750 MHz	50 dB down					
799.9 MHz	850 MHz	50 dB down					
2000 MHz	1950 MHz 2050 MHz	64 dB down 64 dB down					
1999.9 MHz	1950 MHz 2050 MHz	64 dB down 64 dB down					
		<5%					
	SPURIOUS SIGNALS (All spurious signals do 80 dB minimum) Step 8 Spurious Responsive Under Test 100.280000 MHz 200.280000 MHz 409.720000 MHz 1109.720000 MHz 1209.720000 MHz 2400.000000 MHz 2400.000000 MHz 2400.000000 MHz 2400.000000 MHz 300.000000 MHz 300.0000000 MHz 300.0000000 MHz 300.0000000000000000000000000000000000	Step 8 Spurious Response	Min. SPURIOUS SIGNALS, NARROWBAND (All spurious signals down from carrier 80 dB minimum) Step 8 Spurious Response System Under Test Reference Unit 100.280000 MHz 200.561000 MHz 80 dB down 409.720000 MHz 409.441000 MHz 80 dB down 109.720000 MHz 109.441000 MHz 80 dB down 1109.720000 MHz 1109.441000 MHz 80 dB down 1209.720000 MHz 1209.441000 MHz 80 dB down 1209.720000 MHz 1209.441000 MHz 80 dB down 1209.720000 MHz 1209.441000 MHz 80 dB down 2400.000000 MHz 2400.101000 MHz 2400.000000 MHz 2400.201000 MHz 2400.000000 MHz 2400.301000 MHz 74 dB down 74 dB down 2400.000000 MHz 2400.401000 MHz 74 dB down 74 dB down 74 dB down 1050 dB, minimum.) Step 2 Spurious Response Mainframe Frequency Spur Frequency 1299 MHz 150 MHz 50 dB down 50 dB down 1050 MHz 50 dB down 1050 MHz 50 dB down 64 dB down 1099.9 MHz 1950 MHz 64 dB down 64 dB down 1099.9 MHz 1950 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 2050 MHz 2050 MHz 64 dB down 64 dB down 2050 MHz 2	Nin. Actual			

Table 4-3. Performance Test Record (7 of 7)

Para.	Took	Results					
No.	Test	Min.	Actual	Max.			
4-31B.	PHASE MODULATION DISTORTION – ALTERNATE PROCEDURE						
	Step 5 300 MHz at 1 MHz Modulation rate 86634A <5% 86635A <5%	26 dB down 26 dB down					
	Step 8 299.9 MHz at 10 MHz rate, 86634A <15%	16.5 dB down					
	1 MHz rate,86635A < 5%	26 dB down					
	Step 13 1900 MHz at 5 MHz rate, 86634A < 7% 1 MHz rate, 86635A < 5%	23.1 dB down 26 dB down					

Model 86603A Adjustments

SECTION V ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section contains adjustment procedures required to assure peak performance of the Model 86603A RF Section. The RF Section should be adjusted after any repair or if the unit, in conjunction with the Frequency Extension Module, fails to meet the specifications listed in Section IV of this manual. Prior to making any adjustments, allow the RF Section to warmup for 30 minutes.

5-3. The order in which some adjustments are made to the RF Section is critical. Perform the adjustments under the conditions presented in this section. Do not attempt to make adjustments randomly to the instrument. Prior to making any adjustments to the RF Section, refer to the paragraph entitled Related Adjustments.

5-4. EQUIPMENT REQUIRED

5-5. Each adjustment procedure in this section contains a list of test equipment and accessories required to perform the adjustment. The test equipment is also identified by callouts in the test setup diagrams included with each procedure.

5-6. If substitutions must be made for the specified test equipment, refer to Table 1-3 for the minimum specifications of the test equipment to be used in the adjustment procedures. Since the Synthesized Signal Generator System is extremely accurate, it is particularly important that the test equipment used in the adjustment procedures meets the critical specifications listed in the table.

5-7. The HP 11672A Service Kit is an accessory item available from Hewlett-Packard for use in maintaining the RF Section. A detailed listing of the items contained in the service kit is provided in the 11672A Operating Note and in Section I of the mainframe manuals. Any item in the kit may be ordered separately.

5-8. SAFETY CONSIDERATIONS

5-9. Although this instrument has been designed in accordance with international safety standards, this manual and the system mainframe manual contain information, cautions, and warnings which must be followed to ensure safe operation and to retain the complete system in safe condition. Service adjustments should be performed only by qualified service personnel.

NOTE

Refer to the mainframe manual for safety information relating to ac line (Mains) voltage, fuses, protective earth grounding, etc.

5-10. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

5-11. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

WARNING

Adjustments described herein are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may constitute a shock hazard.

5-12. FACTORY SELECTED COMPONENTS

5-13. Factory selected components are identified on the schematics and parts list by an asterisk which follows the reference designator. The normal value of the components are shown. The manual change sheets will provide updated information pertaining to the selected components. Table 5-1 lists the reference designator, the criterion used for selecting a particular value, the normal value range, and the service sheet where the component part is shown.

5-14. RELATED ADJUSTMENTS

5-15. The RF Output Level and 1 dB Step Attenuator Adjustments interact. The Amplitude Modulation Input Circuit Adjustment is dependent on and should be performed after the previously mentioned Adjustments. The Phase Modulation Level and Distortion Adjustment is affected by and should be performed after the Phase Modulator Driver Frequency Response Adjustment. All other adjustments are independent.

5-16. If the RF Output Level Adjustment is performed, the 1 dB Step Attenuator Adjustment should follow immediately. Repeat these procedures until the RF levels are within the stated limits without further adjustment. Then perform the Amplitude Modulation Input Circuit Adjustment. If the Phase Modulator Driver Frequency Response Adjustment is performed, the Phase Modulation

Level and Distortion Adjustment should be performed.

5-17. If the RF Output Level and 1 dB Step Attenuator Adjustments are not performed, the Amplitude Modulation Input Circuit Adjustment may be considered independent. If the Phase Modulator Driver Frequency Response Adjustment is not performed, the Phase Modulation Level and Distortion Adjustment may be considered independent.

If the RF Section is reinserted into the mainframe for adjustments, the mainframe top and/or right side covers must be removed. Refer to the left-hand foldout page immediately preceding the last foldout in this manual for procedures explaining how to remove the RF Section from the mainframe, the RF Section cover removal, and how to interconnect the RF Section and mainframe for adjustments.

Table 5-1. Factory Selected Components

Reference Designator	Selected For	Normal Value or Range	Service Sheet
A4R17	Accurately set the 10 dB difference in the power output between OUTPUT RANGE switch settings of +10 and 0 dBm (the VERNIER control is not moved). Increasing the values will increase the difference.	237Ω	6
A16R5	Sets the adjustment range of the Gain Tracking Control A16R4. Refer to the Phase Modulator Driver Adjustments Procedure.	10-316Ω	5
A21R26	Sets offset current level for A21U7 so that fine tune adjustments will have full travel.	100K-300KΩ	10
A21R36	Limits current in R1, R2, and R3 of the 50 MHz High Pass Filter. Measure the voltage (Vdc) to ground at the junction of A7L1 and A7C1. If Vdc ≤ 11.0, no resistor is needed. If 11.0 < Vdc < 14.0, select a 1.96K resistor. If Vdc ≥ 14.0, select a 1.0K resistor.	None to 1.96KΩ	10

CAUTION

The Model 86603A RF Section, when used with early model mainframes, has -32 Vdc exposed on the A20 Assembly and on Q1 whenever the mainframe LINE switch is set to STBY. During adjustment and maintenance, do not contact these parts with metal tools. Damage can occur to the mainframe power supply, the A20 Assembly and/or Q1. Models 8660A and 8660C with serial prefixes 1508A and below, and all 8660B's have this characteristic.

NOTE

It may be necessary to remove the upper guide rail to gain access to some of the adjustable components.

5-18. ADJUSTMENT LOCATIONS

5-19. The last foldout in this manual contains a table which cross-references all pictorial and schematic locations of the adjustable controls. The figure accompanying the table shows the locations of adjustable controls, assemblies, and chassismounted parts.

5-20. ADJUSTMENTS

5-21. Before performing the adjustment procedures (1) disconnect the mainframe (Mains) Power Cable, (2) remove the RF Section from the mainframe, and (3) remove the RF Section covers. At this point, the RF Section is either reinserted into the mainframe of connected to the mainframe with interconnection cables supplied in the Service Kit.

5-22. POST ADJUSTMENT TESTS

5-23. After adjustments are performed verify that the system performance is within the parameters specified for the RF Section and Frequency Extension Module. Perform the applicable performance test(s) found in Section IV.

WARNING

The multi-pin plug connector (on mainframe), which provides interconnection to the RF Section, will expose power supply voltages which may remain on the pins after the RF Section is removed and after the (Mains) power cable is disconnected from the mainframe. Be careful to avoid contact with the pins during interconnection with the RF Section.

5-24. RF OUTPUT LEVEL ADJUSTMENT

REFERENCE:

Service Sheet 6.

DESCRIPTION:

The Meter and Detector Bias controls are adjusted alternately at specific RF Output levels until the VER-NIER'S control of the RF Output is linear across the control range.

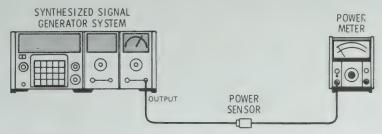


Figure 5-1. RF Output Level Adjustment Test Setup

EQUIPMENT:

PROCEDURE:

NOTE

Prior to performing the procedure, clean the meter face with antistatic glass cleaner.*

- 1. Extract the RF Section from the mainframe. Remove the mainframe top cover and the RF Section covers. Insert the RF Section into the mainframe.
- 2. Zero the external Power Meter.
- 3. Interconnect the equipment as illustrated in Figure 5-1.
- 4. Set the system center frequency to 1000 MHz and the OUTPUT RANGE switch to the 0 dBm position.
- 5. Adjust the VERNIER control for a +3.5 dBm indication on the external Power Meter.
- 6. Adjust the MTR potentiometer A4R26 for a +3.0 dB indication on the front panel meter.
- 7. Adjust the VERNIER control for a front panel meter indication of -6.0 dB.
- 8. Adjust the BIAS potentiometer A4R13 for a -5.5 dBm indication on external Power Meter.
- 9. Repeat steps 5 through 8 until the RF Section's front panel meter indicates power levels that are within ±0.3 dB of the external Power Meter indication with no further adjustment.

5-24. RF OUTPUT LEVEL ADJUSTMENT (Cont'd)

NOTE

The output level is offset by 0.5 dB in this prodedure. This ensures the output level is centered on the selected value over the entire frequency range.

5-25. 1 dB STEP ATTENUATOR ADJUSTMENT

REFERENCE:

Service Sheet 8.

DESCRIPTION:

RF Level and RF Linearity controls are adjusted alternately at specific RF Output levels until the programmed 1 dB step control of RF Output is linear across the range (10 dB).

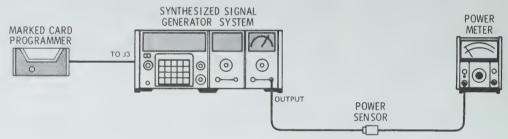


Figure 5-2. 1 dB Step Attenuator Adjustment Test Setup

EQUIPMENT:

- 1. Connect the equipment as illustrated in Figure 5-2.
- 2. Zero the external Power Meter.
- 3. Use a Marked Card Programmer to program the mainframe for a center frequency of 1000 MHz and the RF Section for an output power level of +3 dBm.
- 4. Adjust the RF Section's RF Level Control A10R7 for a +3.5 dBm indication on power meter.
- 5. Use the Marked Card Programmer to program the RF Section for an output power level of -6 dBm.
- 6. Adjust the Linearity control A3R4 for a -5.5 dBm indication on the power meter.
- 7. Repeat steps 3 through 6 until the programmed output power levels are within ± 0.3 dB of the required power meter indication.
- 8. Recheck the power meter readings for the RF Output Level Adjustments. If necessary, perform the adjustments again. Then check the power meter readings for this procedure. Alternately perform one procedure and check the power meter readings on the other until the RF levels are within tolerance without further adjustment.

Model 86603A Adjustments

ADJUSTMENTS

5-25. 1 dB STEP ATTENUATOR ADJUSTMENT (Cont'd)

9. Perform the Amplitude Modulation Input Circuit Adjustments.

5-26. AMPLITUDE MODULATION INPUT CIRCUIT ADJUSTMENT

REFERENCE:

Service Sheet 8.

DESCRIPTION:

A specific modulation drive level is coupled to the RF Section. The RF output signal is demodulated by a peak detector in a spectrum analyzer (when the frequency-span width is set to zero). The ac and dc components are measured with a voltmeter at the detector (vertical) output. First, the dc component is set to -283 mVdc plus the detector offset correction. Then, the ac component is measured. The AM level (%) is 1/2 (one half) the rms output.

Because of the required measurement accuracy, the accuracy of the spectrum analyzer's detector offset must be known to ±2 mVdc. The offset voltage is calculated by measuring the change in the detector output for a change in the RF input and assuming a linear detector over the range of the levels used.

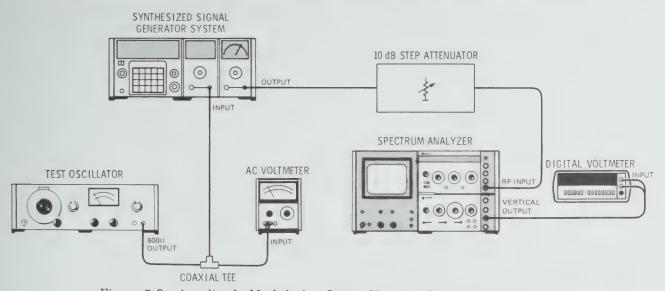


Figure 5-3. Amplitude Modulation Input Circuit Adjustment Test Setup

EQUIPMENT:

Test Oscillator								HP 651B
AC Voltmeter								
10 dB Step Attenuator						۰	٠	HP H38-355D
Spectrum Analyzer								HP 8555A/8552B/140T
Digital Voltmeter								
Coaxial Tee (2 required)								
Crystal Detector								
Oscilloscope				۰				HP 180C/1801A/1821A
Resistor, 1K								

5-26. AMPLITUDE MODULATION INPUT CIRCUIT ADJUSTMENT (Cont'd)

PROCEDURE:

- 1. Remove the RF Section from the mainframe. Remove the mainframe top cover and the RF Section covers. Insert the RF Section into the mainframe.
- 2. Connect the equipment as shown in Figure 5-3.
- 3. Set the synthesized signal generator controls as follows: center frequency 30 MHz, OUTPUT RANGE 0 dBm, VERNIER control for a panel meter reading of +3 dB, and AM off.
- 4. Let the spectrum analyzer warm up for 1 hour to minimize drift of the spectrum analyzer detector output. Set the 10 dB attenuator to 10 dB attenuation.
- 5. Set the spectrum analyzer center frequency to 30 MHz, frequency span per division 5 MHz, resolution bandwidth 300 kHz; input attenuation to 20 dB, and vertical sensitivity per division 10 dB. Adjust the center frequency control to center the display. Set the frequency span to zero and tune to peak the trace.

NOTE

Throughout this test, continually check that the signal is peaked for maximum deflection. Tune the center frequency control for maximum signal deflection.

6.	Set the vertical scale to linear and adjust the reference level vernier for a digital voltmeter reading of
	-200 mVdc.

7.	Set the 10 d	B step attenuator to 0	dB and record th	e digital voltmeter reading.

____mVdc

8. Set the 10 dB step attenuator to 20 dB and record the digital voltmeter reading.

____mVdc

9. Calculate the offset voltage using the following formula:

$$V_{\text{off}} = \frac{\text{mVdc} + 200\alpha}{1 - \alpha}$$

where

 $V_{\rm off}$ is the offset voltage in millivolts mVdc is the DVM reading in millivolts. α is 3.16 (step 7) and 0.316 (step 8).

For example:

mVdc = -687 in step 7

therefore
$$V_{off} = \frac{-687 + 200 (3.16)}{1 - (3.16)} = +25.5 \text{ mVdc}$$

10. Find the value of $V_{\rm off}$ for step 8. The difference between the two should be <4 mVdc. Use the average value of $V_{\rm off}$.

 $V_{off} = ___m Vdc$

11. Set the 10 dB step attenuator to 10 dB.

5-26. AMPLITUDE MODULATION INPUT CIRCUIT ADJUSTMENT (Cont'd)

- 12. Set the system center frequency to 1000 MHz, the modulation mode to AM, the modulation source to external, and a modulation level of 50% (0.5 Vrms input to an Auxiliary Section) at a 1 kHz rate.
- 13. Set the spectrum analyzer center frequency control to 1000 MHz, and set the reference level vernier for a digital voltmeter reading of -283 mVdc + V_{Off}. See Step 10.
- 14. Set the DVM controls to measure the peak detector's ac component. The modulation level (%) is 1/2 (one-half) the DVM reading (Vrms). Adjust the AM CAL Control A10R5 for a reading of 100 mVrms.
- 15. Set the RF Section's VERNIER control for a front panel meter reading of -6 dB.
- 16. Set the DVM to monitor the dc vertical output. Reset the DVM reading of -283 mVdc + Voff.
- 17. Set the DVM to monitor the ac vertical output. Adjust the AM Linearity control A10R2 for a DVM reading of 100 mVrms.
- 18. Repeat steps 13 through 17 until the DVM reading is 100 ±2 mVrms at RF Section meter readings of +3 and -6 dB without further adjustment.

5-27. DOUBLER POWER SUPPLY ADJUSTMENT

REFERENCE:

Service Sheet 12.

DESCRIPTION:

A digital voltmeter monitors the output while the DOUBLER VOLTAGE control is adjusted for the correct output voltage.

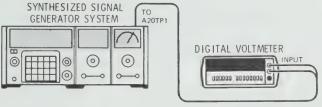


Figure 5-4. Doubler Power Supply Adjustment Test Setup

EQUIPMENT:

- 1. Remove the RF Section from the mainframe. Remove the mainframe top cover and the RF Section covers. Insert the RF Section into the mainframe.
- 2. Connect the digital Voltmeter probe to A20TP1.
- 3. Set the system center frequency ≥ 1300 MHz.
- 4. Adjust the DOUBLER VOLTAGE control (A20R7) for an indication of +22.0 ±0.1 Vdc.

5-28. FILTER DRIVER ASSEMBLY ADJUSTMENT

REFERENCE:

Service Sheet 10.

DESCRIPTION:

A Digital Voltmeter is used to monitor the Filter Driver Assembly output. Adjustable pretune controls are set for specified output voltages at specific center frequencies.

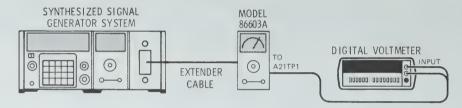


Figure 5-5. Filter Driver Assembly Adjustment Test Setup

EQUIPMENT:

- 1. Remove the RF Section from the mainframe. Remove the RF Section covers.
- 2. Connect the equipment as shown in Figure 5-5.
- 3. Set the mainframe center frequencies and adjust the pretune controls to the correct output voltage at A21TP1 as shown in Table 5-2.

Model 86603A Adjustments

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5-28. FILTER DRIVER ASSEMBLY ADJUSTMENT (Cont'd)

Table 5-2. Center Frequency versus Filter Driver Output

Center Frequency	Pretune Control	A21TP1 (Vdc)				
(MHz)	Control	Min.	Max.			
1300	A21R7	-0.19	-0.23			
2599	A21R13	-33.0	-37.0			
1300	A21R7	-0.19	-0.23			
1400	A21R1	-0.50	-0.70			
1600	A21R2	-1.6	-2.0 ·			
1800	A21R3	-3.4	-4.2			
2000	A21R4	-5.8	-6.9			
2200	A21R5	-9.5	-10.5			
2400	A21R6	-17.5	-19.5			
1500	A21R8	-1.0	-1.2			
1700	A21R9	-2.5	-2.9			
1900	A21R10	-4.5	-5.5			
2100	A21R11	-7.5	-8.5			
2300	A21R12	-12.3	-13.7			

5-29. PHASE MODULATOR DRIVER FREQUENCY RESPONSE ADJUSTMENTS

REFERENCE:

Service Sheet 5

DESCRIPTION:

The output of a sweep generator is connected to the A16 Phase Modulator Driver Assembly input while a spectrum analyzer monitors the system's phase modulated RF output. The frequency response control is adjusted for maximum flatness to ±40 MHz and for minimum peaking at 80 MHz.

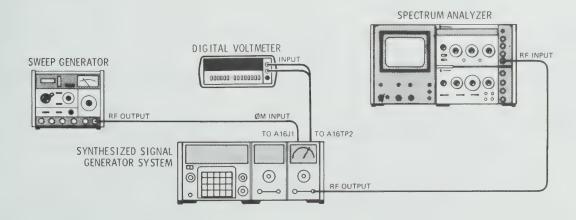


Figure 5-6. Phase Modulator Driver Frequency Response Adjustment Test Setup

5-29. PHASE MODULATOR DRIVER FREQUENCY RESPONSE ADJUSTMENTS (Cont'd)

EQUIPMENT:

Sweep Generator HP 8601A

Digital Voltmeter. HP 3466A

- 1. Remove the RF Section from the mainframe. Remove the mainframe top cover and the RF Section covers and top guide rail.
- 2. Remove cable W12 from the ϕ M Input A16J1 and wrap the connector with insulating tape. Connect 11672-60005 (from the Service Kit) to A16J1. Route the BNC end of cable into the cavity and out through the top of the mainframe. Carefully reinstall the RF Section so as not to damage the cables.
- 3. Set the sweep generator controls as follows: sweep range to 110 MHz, frequency to 100 MHz, output level to -10 dBm, sweep the video, sweep mode to free-slow, and sweep vernier fully clockwise.
- 4. Connect the equipment as shown in Figure 5-6.
- 5. Set the synthesized signal generator controls for a center frequency of 1.05 GHz and an output level of 0 dBm.
- 6. On the spectrum analyzer, set the controls for center frequency of 1.05 GHz, frequency span per division of 20 MHz, resolution bandwidth to 300 kHz, input attenuation of 30 dB, vertical sensitivity per division linear, and sweep time per division at 2 ms.
- 7. On the RF section, center the Gain Tracking Adj control (A16R27).
- 8. Set the Second Harmonic Adj control for +7.0 Vdc on A16TP2.
- 9. Remove the DVM connection to A16TP2.
- 10. Set the Third Harmonic control (A16R1) and the Gain Adj control (A16R2) to fully counterclockwise positions.
- 11. Adjust the sweep generator output level until the sidebands are approximately 34 dB below the carrier level.
- 12. Adjust the Frequency Response Control (A16C7) for maximum flatness within 40 MHz of the carrier and for minimum peaking at frequencies from 60 to 80 MHz.
- 13. Disconnect the sweep generator from the A16 Assembly. On the signal generator, set the LINE switch to STBY.
- 14. Carefully remove the RF Section as damage to the cables could occur. Reconnect W12 to A16J1.

5-30A. PHASE MODULATION LEVEL AND DISTORTION ADJUSTMENTS

REFERENCE:

Service Sheet 5.

DESCRIPTION:

The phase modulated signal from the synthesized signal generator is monitored by a spectrum analyzer and is adjusted to the modulation level indicated by the modulation level meter. The phase modulated signal is then demodulated by the modulation analyzer and the modulation output is connected to the spectrum analyzer. The adjustments are set to minimize harmonic distortion. The modulation level and distortion adjustments are repeated until both are within the required accuracy.

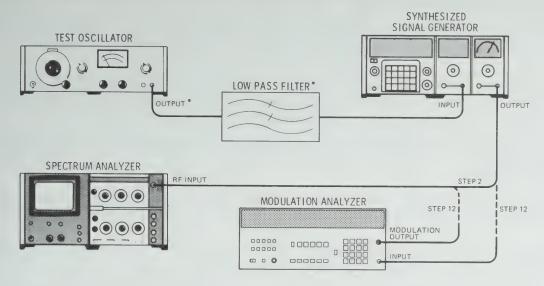


Figure 5-7A. Phase Modulation Level and Distortion Adjustment Test Setup

EQUIPMENT:

Spectrum Analyzer.			۰				٠		۰	٠		HP 8553B/8552B/140T
Test Oscillator												HP 651B
Modulation Analyzer											٠	HP 8901A
Low Pass Filters (100	k	Hz	at	50	Ω	or	60	0Ω	2)	٠		Special (see Figure 1-2)

- 1. Extract the RF Section from mainframe. Remove the mainframe top cover, the RF Section covers, and the top guide rail. Insert the RF Section back into the mainframe.
- 2. Connect the equipment as shown in Figure 5-7A. Connect the output of the signal generator directly to the spectrum analyzer RF input. Be sure to use the correct impedance test oscillator output and the correct low pass filter.
- 3. Set the test oscillator output to 100 kHz at 1.5 Vrms.
- 4. Set the signal generator center frequency to 100 MHz with 0 dBm OUTPUT level.

^{*}In Figure 5-7A, the test oscillator output and low pass filter impedances are 50Ω when the modulation section being used is a Model 86634A and 600Ω when used with an 86635A.

5-30A. PHASE MODULATION LEVEL AND DISTORITON ADJUSTMENTS (Cont'd)

- 5. Set the spectrum analyzer controls for a center frequency of 100 MHz, resolution bandwidth of 10 kHz, frequency span per division of 0.5 MHz, sweep time per division of 10 ms, input attenuation of 30 dB, vertical scale per division to 2 dB and adjust the reference level to a readable level.
- 6. Set the Modulation Section controls for Φ M mode, external AC source, and a modulation level of exactly 82° as read on the front panel meter.
- 7. Adjust A16R2 so the carrier and first sidebands are of equal amplitude.
- 8. Step the System Under Test center frequency down 1 Hz to 99.999 999 MHz. Adjust A16R27 so the carrier and first sidebands are equal.
- 9. Set the Modulation Analyzer to AUTOMATIC OPERATION and FM mode. Switch in the 300 Hz HP filter.
- 10. Set the spectrum analyzer controls for a center frequency of 100 kHz, resolution bandwidth to 3 kHz, frequency span per division 100 kHz, input attenuation to 0 dB, log reference level to a convenient level, vertical sensitivity per division to 10 dB, and scan time per division to 20 ms.
- 11. Set the signal generator center frequency to 100 MHz; set the modulation level to 100° as read on the front panel meter.
- 12. Refer to Figure 5-7A and connect the signal generator output to the Modulation Analyzer input. Connect the Modulation Analyzer MODULATION OUTPUT to the spectrum analyzer RF input.
- 13. Adjust the spectrum analyzer's reference level control so the peak of the fundamental 100 kHz signal is viewed on the CRT dispaly at the log reference graticule line.
- 14. Adjust A16R36 to null the second harmonic level; adjust A16R1 to null the third harmonic level.

NOTE

Observing harmonic distortion of a ΦM signal after passing it through an FM discriminator results in an increase in level of 6 dB per octave. Therefore, the measured second harmonic level will be 6 dB higher and the third harmonic level 9.5 dB higher than with a phase demodulator.

- 15. Step the signal generator center frequency down 1 Hz. Note the direction and amount of readjustment of A16R36 and R1 necessary to null the second and third harmonics.
- 16. Set A16R36 and R1 for the best compromise (minimum second and third harmonic levels) at both center frequency settings of 99.999 999 and 100.000 000 MHz.
- 17. Set the signal generator center frequency to 100 MHz; set the modulation level to 82 degrees as indcated on the Modulation Section meter.
- 18. Reconnect the signal generator output directly to the spectrum analyzer input.
- 19 Adjust A16R2 for equal carrier and first sideband levels.

5-30A. PHASE MODULATION LEVEL AND DISTORTION ADJUSTMENTS (Cont'd)

- 20. Step center frequency down 1 Hz to 99.999 999 MHz and adjust A16R27 for equal amplitude carrier and first sidebands.
- 21. Repeat steps 4 through 20 until all the conditions below are met without further adjustment.
 - a. Carrier and first sidebands are equal within 0.5 dB when changing Center Frequency of System Under Test between 100 and 99.999 999 MHz (Steps 7-8).
 - b. Second harmonic levels are equal within 4 dB or >40 dB down from the fundamental as indicated by the spectrum analyzer at center frequencies of 100 and 99.999 999 MHz (Step 17).
 - c. Third harmonic levels are equal within 4 dB > 35 dB down from the fundamental as indicated by the spectrum analyzer at center frequencies of 300 and 299.999 999 MHz (Step 17).
- 22. Replace the RF Seciton top guide rail and covers, and the mainframe cover.

5-30B. PHASE MODULATION LEVEL AND DISTORTION ADJUSTMENTS - ALTERNATE PROCEDURE

REFERENCE:

Service Sheet 5.

DESCRIPTION:

The phase modulated signal from the synthesized signal generator is monitored by a spectrum analyzer and is adjusted to the modulation level indicated by the modulation level meter. The phase modulated signal is then mixed down, the difference frequency is connected to a phase demodulator, and the detected output is connected to the spectrum analyzer. The adjustments are set to minimize harmonic distortion. The modulation level and distortion adjustments are repeated until both are within the required accuracy.

5-30B. PHASE MODULATION LEVEL AND DISTORTION ADJUSTMENTS - ALTERNATE PROCEDURE (Cont'd)

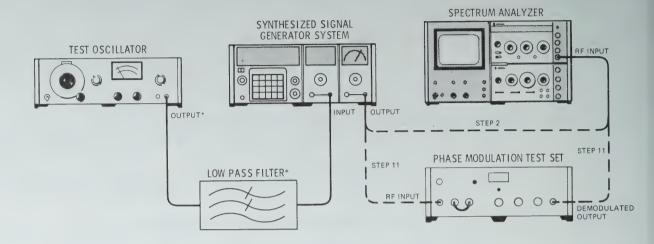


Figure 5-7B. Phase Modulation Level and Distortion Adjustment Test Setup (Alternate Procedure)

EQUIPMENT:

- 1. Extract the RF Section from mainframe. Remove the mainframe top cover, the RF Section covers, and the top guide rail. Insert the RF Section back into the mainframe.
- 2. Connect the equipment as shown in Figure 5-7B. Connect the output of the System Under Test directly to the spectrum analyzer RF input. Be sure to use the correct impedance test oscillator output and the correct low pass filter*.
- 3. Set the test oscillator output to 100 kHz at 1.5 Vrms.
- 4. Set the System Under Test center frequency to 100 MHz with a 0 dBm OUTPUT level.
- 5. Set the spectrum analyzer controls for a center frequency of 100 MHz, resolution bandwidth of 10 kHz, frequency span per division of 0.5 MHz, sweep time per division of 10 ms, input attenuation of 30 dB, vertical scale per division of 2 dB, and adjust the reference level to a readable level.
- 6. Set the Modulation Section controls for ϕ M mode, external AC source, and a modulation level of exactly 82 degrees as read on the front panel meter.
- 7. Adjust A16R2 so the carrier and first sidebands are of equal amplitude.

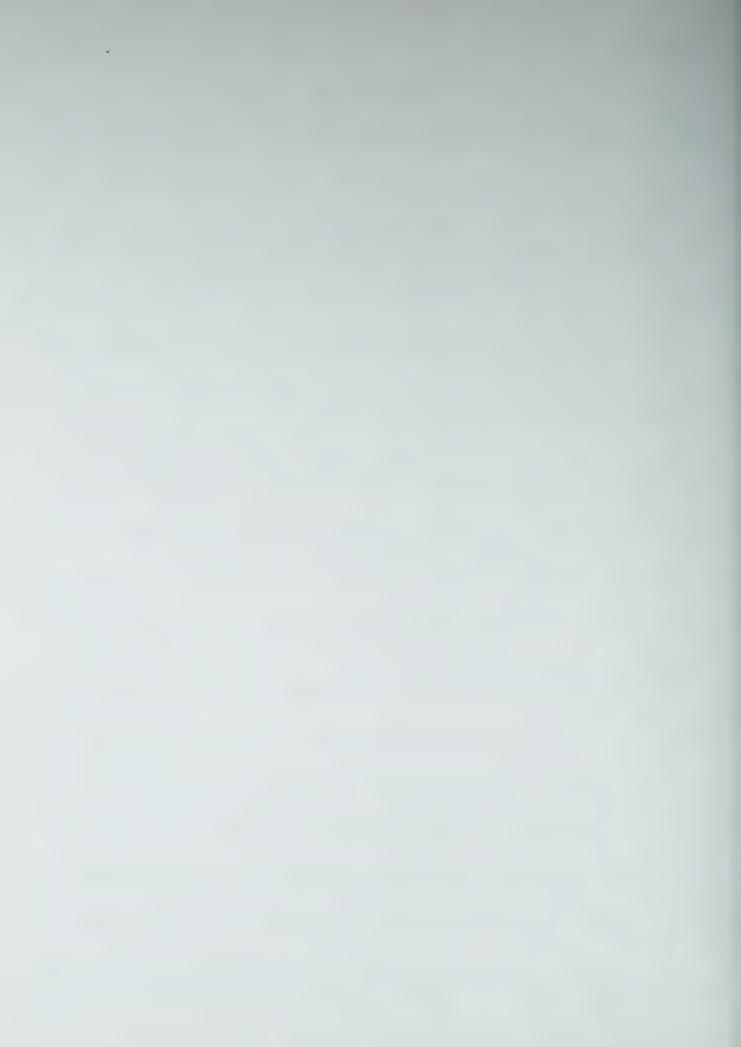
^{*}In Figure 5-7B the test oscillator output and low pass filter impedances are 50 ohms when the modulation section being used is a Model 86634A and 600 ohms when used with an 86635A.

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ADJUSTMENTS

5-30B. PHASE MODULATION LEVEL AND DISTORTION ADJUSTMENTS - ALTERNATE PROCEDURE (Cont'd)

- 8. On the System Under Test, step the center frequency down 1 Hz to 99.999999 MHz. Adjust A16R27 until the carrier and first sidebands are equal.
- 9. On the spectrum analyzer, set the controls for a center frequency of 2 MHz, a resolution bandwidth to 30 kHz, frequency span per division to 0.5 MHz, input attenuation to 30 dB, log reference level to a convenient level, vertical sensitivity per division to 10 dB, and scan time per division to 10 ms.
- 10. On the System Under Test, set the center frequency to 300 MHz with a modulation level of 100 degrees as read on the front panel meter.
- 11. Connect the phase modulation test set between the signal generator output and the spectrum analyzer input as shown in Figure 5-7B.
- 12. Adjust the reference level on the spectrum analyzer until the peak of the fundamental 1 MHz signal is viewed on the CRT display at the log reference graticule line.
- 13. Adjust A16R36 to null the second harmonic level; adjust A16R1 to null the third harmonic level.
- 14. On the System Under Test, step the center frequency down 1 Hz. Note the direction and amount of readjustment of A16R36 and R1 necessary to null the second and third harmonics.
- 15. Set A16R36 and R1 for the best compromise (minimum second and third harmonic levels) at both center frequency settings of 299.99999 and 300 MHz.
- 16. On the System Under Test, set the center frequency to 100 MHz; set the modulation level to 82 degrees as indicated on the Modulation Section meter.
- 17. Reconnect the RF Section output directly to the spectrum analyzer input.
- 18. Adjust A1R2 for equal carrier and first sideband levels.
- 19. Step the center frequency down 1 Hz to 99.999999 MHz and adjust A16R27 for equal amplitude carrier and first sidebands.
- 20. Repeat steps 4 through 20 until all the following conditions are met without further adjustment.
 - a. When changing the center frequency of the System Under Test between 100 and 99.999999 MHz (steps 7 and 8), the carrier and first sideband should be equal within 0.5 dB.
 - b. Second harmonic levels are equal within 4 dB or >46 dB down from the fundamental at center frequencies of 300 and 299.999999 MHz (step 15).
 - c. Third harmonic levels are equal within 4 dB or >46 dB down from the fundamental at center frequencies of 300 and 299.99999 MHz (step 15).
- 21. Replace the RF section top guide rail and covers and the mainframe cover.



Model 86603A Replaceable Parts

SECTION VI REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. Table 6-1 is a list of exchange assemblies, and Table 6-2 lists abbreviations used in the parts list and throughout the manual. Table 6-3 lists all replaceable parts in reference designator order. Table 6-4 contains the names and addresses that correspond to the manufacturer's code numbers.

6-3. EXCHANGE ASSEMBLIES

6-4. Table 6-1 lists assemblies within the instrument that may be replaced on an exchange basis, thus affording a considerable cost saving. Exchange, factory-repaired and tested assemblies are available only on a trade-in basis; therefore, the defective assemblies must be returned for credit. For this reason, assemblies required for spare parts stock must be ordered by the new assembly part number.

6-5. ABBREVIATONS

6-6. Table 6-2 lists abbreviations used in the parts list, schematics and throughout the manual. In some cases, two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower case and upper case letters.

6-7. REPLACEABLE PARTS LIST

- 6-8. Table 6-3 is the list of replaceable parts and is organized as follows:
- a. Electrical assemblies and their components in alpha-numerical order by reference designation.
- b. Chassis-mounted parts in alphanumerical order by reference designation.
 - c. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number.

- b. Part number check digit (CD).
- c. The total quantity (Qty) found in the instrument.
 - d. The description of the part.
- e. Typical manufacturer of the part in a five-digit code.
- f. Manufacturer's code number for the part. The total quantity for each part is given only once at the first appearance of the part number in the list.

6-9. ORDERING INFORMATION

- 6-10. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.
- 6-11. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-12. SPARE PARTS KIT

6-13. Stocking spare parts for an instrument is often done to ensure quick return to service after a malfunction occurs. Hewlett-Packard has a "Spare Parts Kit" available for this purpose. The kit consists of selected replaceable assemblies and components for this instrument. The contents of the kit and the "Recommended Spares" list are based on failure reports and repair data, and parts support for one year. A Recommended Spares list or the Spare Parts Kit (which contains the list) may be ordered through your nearest Hewlett-Packard office.

6-14. DIRECT MAIL ORDER SYSTEM

- 6-15. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:
- a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

Replaceable Parts Model 86603A

- No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).
- Prepaid transportation (there is a small handling charge for each order).
- d. No invoices to provide these advantages, a check or money order must accompany each order.
- 6-16. Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Part Numbers for Exchange Assemblies

Reference	Description -	Part Number*			
Designation	Description	Exchange Assembly	New Assembly		
A13	Attenuator Assembly	86601-60109	86603-60043		
A22	Frequency Doubler Assembly	86603-60054	86603-60053		

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A								
A assembly								
AT attenuator; isolator;								
termination								
B fan; motor								
BT battery								
C capacitor								
CP coupler								
CR diode; diode								
thyristor; varactor								
DC directional coupler								
DL delay line								
DS annunciator;								
signaling device								
(audible or visual);								
lamp; LED								

E miscellaneous									
electrical part									
F fuse									
FL filter									
H hardware									
HY circulator									
J electrical connector									
(stationary portion);									
jack									
K relay									
L coil; inductor									
M meter									
MP miscellaneous									
mechanical part									

D								
P		٠	۰		e	le	C	trical connector
					(1	m	01	vable portion);
					p	lu	ıg	
Q		۰		۰	٠	۰		transistor: SCR:
					Ù	i	od	de thyristor
R	٠		٠	۰	۰			resistor
R	r			٠	٠	۰	٠	thermistor
S		۰			۰	۰	٠	switch
T	۰	٠			٠			transformer
TH	3		٠		٠	۰	٠	terminal board
TO	3							thermocouple
								test point

U integrated circuit;
microcircuit
V electron tube
VR voltage regulator;
breakdown diode
W cable; transmission
path; wire
X socket
Y crystal unit (piezo-
electric or quartz)
Z tuned cavity; tuned
circuit

ABBREVIATIONS

A ampere
ac alternating current
ACCESS accessory
ADJ adjustment
A/D analog-to-digital AF audio frequency
AF audio frequency
AFC automatic
frequency control
AGC automatic gain
control
AL aluminum
ALC automatic level
control
AM amplitude modula-
tion
AMPL amplifier
APC automatic phase
control
ASSY assembly
AUX auxiliary
avg average
AWG American wire
gauge
BAL balance
BCD binary coded
decimal
BD board
BE CU beryllium
copper
BFO beat frequency
BFO beat frequency oscillator
BFO beat frequency oscillator
BFO beat frequency oscillator
BFO beat frequency oscillator BH binder head BKDN breakdown BP bandpass
BFO beat frequency oscillator BH binder head BKDN . breakdown BP bandpass BPF bandpass filter
BFO beat frequency oscillator BH binder head BKDN . breakdown BP bandpass BPF bandpass filter
BFO beat frequency oscillator BH binder head BKDN . breakdown BP bandpass BPF . bandpass filter BRS brass BWO backward-wave
BFO beat frequency oscillator BH binder head BKDN breakdown BP bandpass Filter BRS brass BWO backward-wave oscillator
BFO beat frequency oscillator BH binder head BKDN breakdown BP bandpass Filter BRS brass BWO backward-wave oscillator
BFO beat frequency oscillator BH binder head BKDN breakdown BP bandpass BPF bandpass filter BRS brass BWO backward-wave oscillator CAL calibrate ccw counter-clockwise
BFO beat frequency oscillator BH binder head BKDN . breakdown BP bandpass Filter BRS brass BWO backward-wave oscillator CAL calibrate ccw . counter-clockwise CER ceramic
BFO beat frequency oscillator BH binder head BKDN . breakdown BP bandpass BPF . bandpass filter BRS brass BWO backward-wave oscillator CAL calibrate ccw . counter-clockwise CER ceramic CHAN channel
BFO beat frequency oscillator BH binder head BKDN breakdown BP bandpass Filter BRS brass BWO backward-wave oscillator CAL calibrate ccw counter-clockwise CER cramic CHAN channel cm centimeter
BFO beat frequency oscillator BH binder head BKDN . breakdown BP bandpass BPF . bandpass filter BRS brass BWO backward-wave oscillator CAL calibrate ccw . counter-clockwise CER ceramic CHAN channel

COEF coefficient
COM common
COMP composition
COMPL
COMPL complete CONN connector
CP cadmium plate
CP cadmium plate CRT cathode-ray tube
CTL complementary
transistor logic
CW continuous wave
cw clockwise
cm centimeter
D/A digital-to-analog
dB decibel
dBm decibel referred
to 1 mW
dc direct current
deg degree (temperature
interval or differ-
o ence)
degree (plane
C degree Celsius
F degree Fahrenheit
K degree Kelvin
DEPC deposited carbon
DET detector
diam diameter
DIA diameter (used in
parts list)
DIFF AMPL differential
amplifier
div division
DPDT double-pole,
double-throw
DR drive
DSB double sideband
DTL diode transistor
logic
DVM digital voltmeter
ECL emitter coupled
logic
EMF electromotive force

EDP electronic data
processing
ELECT electrolytic ENCAP encapsulated
ENCAP encapsulated
EXT external
F farad
FET field-effect
transistor
F/F flip-flop FH flat head
FH flat head
FIL H fillister head
FM frequency modulation
FM frequency modulation
FP front panel FREQ frequency
FREQ frequency
FXD fixed
g gram
CF
GHz gigahertz
GL glass
GRD ground(ed)
H henry
h hour
h hour
h hour HET heterodyne HEX hexagonal
HEX hexagonal
HD head
HDW hardware
HD head HDW hardware HF high frequency
HG mercury HI high
HI high
HP Hewlett-Packard
HPF high pass filter
HPF high pass filter HR hour (used in
parts list)
HV high voltage
Hz Hertz
IC integrated circuit
ID inside diameter
IF intermediate
frequency
IMPG impregnated
in inch
INCD incandescent
INCL include(s)
INCL include(s) INP input
INC imput
INS insulation

INT interna	1
kg kilogram	1
kHz kilohertz	,
kHz kilohertz k Ω kilohm	
kV kilovoli	
kV kilovoli lb pound	i
LC inductance	
capacitance	
LED light-emitting diode	
LIM limit	,
LIN linear taper (used	į
in parts list)	
lin linear	1
LK WASH lock washer	
LO low; local oscillator	ľ
LOG logarithmic taper	
(used in parts list))
log logrithm(ic))
LPF low pass filter	î
LV low voltage	à
m meter (distance))
mA milliampere	,
MAX maximum	ı
${ m M}\Omega$ megohm	
MEG meg (10^6) (used	i
in parts list)	
MET FLM metal film	
MET OX metallic oxide	
MF medium frequency	
microfarad (used in	
parts list)	
MFR manufacturer	
mg milligram	
MHz megahertz	
mho mho	
MIN minimum	
min minute (time)' minute (plane	
' minute (plane	
angle) MINAT miniature mm millimeter	
MINAT miniature	
mm millimeter	

NOTE

All abbreviations in the parts list will be in upper-case.

Table 6-2. Reference Designations and Abbreviations (cont'd)

MOD modulatan	OD autoida diamatar	PWV peak working	TD time dela
MOD modulator	OD outside diameter		
MOM momentary	OH oval head	voltage	TERM termin
MOS metal-oxide	OP AMPL operational	RC resistance-	TFT thin-film transist
semiconductor	amplifier	capacitance	TGL togg
ms millisecond	OPT option	RECT rectifier	THD threa
MTG mounting	OSC oscillator	REF reference	THRU through
MTR meter (indicating	OX oxide	REG regulated	TI titaniu
device)	oz ounce	REPL replaceable	TOL toleran
mV millivolt	Ω ohm	RF radio frequency	TRIM trimm
mVac millivolt, ac	P peak (used in parts	RFI radio frequency	TSTR transist
mvac mmnvoit, ac	list)	interference	TTL transistor-transist
mVde millivolt, de			logic
mVpk millivolt, peak	PAM pulse-amplitude	RH round head; right	
mVp-p millivolt, peak-	modulation	hand	TV televisio
to-peak	PC printed circuit	RLC resistance-	TVI television interferen
mVrms millivolt, rms	PCM pulse-code modula-	inductance-	TWT traveling wave tu
mW milliwatt	tion; pulse-count	capacitance	U micro (10 ⁻⁰) (us
MUX multiplex	modulation	RMO rack mount only	in parts list)
MY mylar	PDM pulse-duration	rms root-mean-square	UF microfarad (used
UA microampere	modulation	RND round	parts list)
	pF picofarad	ROM read-only memory	UHF ultrahigh frequen
UF microfarad	PH BRZ phosphor bronze	R&P rack and panel	UNREG unregulat
UH microhenry			
Umho micromho	PHL Phillips	RWV reverse working	V
Us microsecond	PIN positive-intrinsic-	voltage	VA voltampe
UV microvolt	negative	S scattering parameter	Vac volts,
UVac microvolt, ac	PIV peak inverse	s second (time)	VAR variat
UVdc microvolt, dc	voltage	" . second (plane angle)	VCO voltage-controll
UVpk microvolt, peak	pk peak	S-B slow-blow (fuse)	oscillator
UVp-p microvolt, peak-	PL phase lock	(used in parts list)	Vdc volts,
to-peak	PLO phase lock	SCR silicon controlled	VDCW volts, dc, worki
UVrms microvolt, rms	oscillator	rectifier: screw	(used in parts lis
μW microwatt	PM phase modulation	SE selenium	V(F) volts, filter
nA nanoampere	PNP positive-negative-	SECT sections	VFO variable-frequen
	positive	SEMICON semicon-	oscillator
NC no connection		ductor	VHF very-high f
N/C normally closed	P/O part of		
NE neon	POLY polystyrene	SHF superhigh fre-	quency
NEG negative	PORC porcelain	quency	Vpk volts, pe
nF nanofarad	POS positive; position(s)	SI silicon	Vp-p volts, peak-to-pe
NI PL nickel plate	(used in parts list)	SIL silver	Vrms volts, r
N/O normally open	POSN position	SL slide	VSWR voltage standi
NOM nominal	POT potentiometer	SNR signal-to-noise ratio	wave ratio
NORM normal	p-p peak-to-peak	SPDT single-pole,	VTO voltage-tun
NPN negative-positive-	PP peak-to-peak (used	double-throw	oscillator
negative	in parts list)	SPG spring	VTVM vacuum-tu
		SR split ring	voltmeter
NPO negative-positive	PPM pulse-position		V(X) volts, switch
zero (zero tempera-	modulation	SPST single-pole,	
ture coefficient)	PREAMPL preamplifier	single-throw	W
NRFR not recommended	PRF pulse-repetition	SSB single sideband	W/ wi
for field replace-	frequency	SST stainless steel	WIV working inver
ment	PRR pulse repetition	STL steel	voltage
NSR not separately	rate	SQ square	WW wirewou
replaceable	ps picosecond	SWR standing-wave ratio	W/O without
ns nanosecond	PT point	SYNC synchronize	YIG yttrium-iron-garr
nW nanowatt	PTM pulse-time	T timed (slow-blow fuse)	Z ₀ characteris
	modulation	TA tantalum	impedance
OBD order by descrip-		mc townserting	tubenance
tion	PWM pulse-width modulation	TC temperature compensating	
	modulation	aampangating	

NOTE

All abbreviations in the parts list will be in upper-case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	1012
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10-1
С	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10-6
n	nano	10^{-9}
p	pico	10-12
f	femto	10-15
a	atto	10-18

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
At	86603-60004	5	1	MODULATOR FILTER ASSY	28480	86503-60004
A1J1 A1J2	0360+1514 0360+1514	7		TERMINAL-STUD SGL-PIN PRESS-MTG TERMINAL-STUD SGL-PIN PRESS-MTG	28480 28480	0360=1514 0360=1514
A1L1 A1L2	9140=0158 9140=0158	6 6	3	COIL-MLD 10H 10% Q#32 .095DX.25LG-NOM COIL-MLD 10H 10% Q#32 .095DX.25LG-NOM	28480 28480	9140=0158 9140=0158
A1P1 A1P2 A1P3 A1P4	1251-3172 1251-3172 1251-3172 1251-3172	7 7 7	4	CONNECTOR-SGL CONT SKT .03-IN-BSC-SZ RND	28480 28480 28480 28480	1251=3172 1251=3172 1251=3172 1251=3172
42	86603-60001	2	1	ALC MOTHER BOARD ASSY	28480	86603=60001
42C1	0160=2204 0160=3457	0 7	2	CAPACITOR-FXD 100PF +-5% 300VDC MICA CAPACITOR-FXD 2000PF +-10% 250VDC CER	28480 28480	0160=2204 0160=3457
A2J1	1250=1255	1	1	CONNECTOR-RF SMB M PC 50-0HM	28480	1250+1255
A 2 K 1	0490=0916	6	9	RELAY-REED 1A 500MA 50VDC SVDC-COIL 10VA	28480	0490-0916
42P2	0362=0063 0362=0063	3	5	CONNECTOR=SGL CONT GDISC=FEM CONNECTOR=SGL CONT GDISC=FEM	28480 28480	0362=0063 0362=0063
A201	1854-0404	0	6	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854=0404
A2R1 A2R2 A2R3 A2R4 A2R5	0698=0084 0757=1060 0757=0441 0698=3405 0757=0438	9 9 8 4 3	1 1 1 1	RESISTOR 2,15% 1% ,125% F TC=0+=100 RESISTOR 196 1% ,5% F TC=0+=100 RESISTOR 8,25% 1% ,125% F TC=0+=100 RESISTOR 422 1% ,5% F TC=0+=100 RESISTOR 5,11% 1% ,125% F TC=0+=100	24546 28480 24546 28480 24546	C4=1/8=T0=2151=F 0757=10=0 C4=1/8=T0=8251=F 0598=3405 C4=1/8=T0=5111=F
42H6 42k7 42k8 42k9	0757-0438 0757-0401 0698-3403 0764-0013	3 0 2 5	2 1 1	RESISTOR 5.11K 1% .125W F TC=0+=100 RESISTOR 100 1% .125W F TC=0+=100 RESISTOR 348 1% .5W F TC=0+=100 RESISTOR 56 5% 2W M9 TC=+-200	24546 24546 28480 28480	C4=1/8=T0=5111=F C4=1/8=T0=101=F 0698=3403 0764=0013
18724	1902-3139	7	1	DIODE=ZNR 8,25v 5x D0+7 PD=,4w TC=+.053x	28480	1902-3139
95 x 9 1 9 95 x 9 3 95 x 9 3	1251=1626 1251=1626 1251=1626	5 5	4	CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480 28480 28480	1251=1626 1251=1626 1251=1626
				AZ MISCELLANEOUS		
	0360-1514	7	53	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1514
Az	86603-60040	9	1	ALC AMPLIFIER ASSY	28480	86603=60040
A 3 C 1 A 3 C 2 A 3 C 3 A 3 C 4 A 3 C 5	0180-0058 0180-0058 0140-0193 0160-2199 0160-2199	2 0 0 0 0	1 2	CAPACITOR=FXD 50UF+75=10% 25VDC AL CAPACITOR=FXD 50UF+75=10% 25VDC AL CAPACITOR=FXD 82PF +=5% 300VDC MICA CAPACITOR=FXD 30PF +=5% 300VDC MICA CAPACITOR=FXD 30PF +=5% 300VDC MICA	56289 56289 72136 28480 28480	30D506G025CC2 30D506G025CC2 DM15E820J0300wV1CR 0160~2199 0160~2199
A3C6 A3C7 A3CA A3CA	0160=0302 0160=3468 0160=2204 0160=2238	5 0 0	1 1	CAPACITOR=FXD .018UF +=10% 200VDC POLYE CAPACITOR=FXD .12UF +=10% 80VDC POLYE CAPACITOR=FXD 100PF +=5% 300VDC MICA CAPACITOR=FXD 1.5PF +=.25PF 500VDC CER	28480 28480 28480	0160=0302 0160=3468 0160=2204 0160=2236
A3CR1 A3CR2 A3CR3 A3CR4	1901-0047 1901-0047 1901-0047 1901-0050	8 8 8	3	DIODE-SWITCHING 20V 75MA 10NS DIODE-SWITCHING 20V 75MA 10NS DIODE-SWITCHING 20V 75MA 10NS DIODE-SWITCHING 80V 200MA 2NS DO-35	28480 28480 28480 28480	1901=0047 1901=0047 1901=0047 1901=0050
A 3 K 1	0490-0916	6		RELAY-REED 14 500MA 50VDC 5VDC-COIL 10VA	28480	0490=0916
A 3 L 2 A 3 L 3	9140-0237 9140-0237 9140-0105	2 3	4	COIL-MLD 200UH 5% Q=65 .1550x.375LG-NOM COIL-MLD 200UH 5% Q=65 .1550x.375LG-NOM COIL-MLD 8.2UH 10% Q=50 .1550x.375LG-NOM	28480 28480 28480	9140 = 0237 9140 = 0237 9140 = 0105
4 3 Q 1 4 3 Q 2 4 3 Q 3 4 3 Q 4 4 3 Q 5	1853-0020 1854-0404 1855-0020 1853-0034 1853-0020	40804	16 1 5	TRANSISTOR PNP SI PD=300MW FT=150MHZ TRANSISTOR NPN SI TO=18 PD=360MW TRANSISTOR J=FET N=CHAN D=MODE TO=18 SI TRANSISTOR PNP SI TO=18 PD=360MW TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480 28480 28480 28480	1853=0020 1854=0404 1855=0020 1853=0034 1853=0020
A 3 G 6 A 3 G 7 A 3 G 8 A 3 G 9 A 3 G 1 O	1853-0034 1854-0404 1854-0404 1853-0034 1854-0221	0 0 0 0	2	TRANSISTOR PNP SI TO-18 PD=360MW TRANSISTOR NPN SI TO-18 PD=360MW TRANSISTOR NPN SI TO-18 PD=360MW TRANSISTOR NPP SI TO-18 PD=360MW TRANSISTOR TO SITO-18 PD=360MW TRANSISTOR-DUAL NPN PD=750MW	28480 28480 28480 28480 28480	1853=0034 1854=0404 1854=0404 1854=0034 1854=0034

Table 6-3. Replaceable Parts

				Table 6-3. Replaceable Parts		
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
43011	1854-0053	5	1	TRANSISTOR NPN 2N2218 SI TO+5 PD#800MW	04713	SN2218
\$ 3 R 1 \$ 3 R 2 \$ 3 R 3 \$ 3 R U \$ 3 R 5	0698-3154 0757-0394 0698-0083 2100-2517 0757-0438	0 0 8 4 3	3 3 17 5	RESISTOR 4,22K 1% ,125W F TC=0+=100 RESISTOR 51,1 1% ,125W F TC=0+=100 RESISTOR 1,96K 1% ,125W F TC=0+=100 RESISTOR=TRMR 50K 10% C SIDE=ADJ 1=TRN RESISTOR 5,11K 1% ,125W F TC=0+=100	24546 24546 24546 30983 24546	C4=1/8=T0=4221=F C4=1/8=T0=51R1=F C4=1/8=T0=1961=F ET50X503 C4=1/8=T0=5111=F
43 N 6 43 N 7 43 N A 43 N 9 43 N 1 0	0757-0482 0757-0416 0757-0438 0757-0442 0757-0438	7 7 3 9 3	3 5	RESISTOR 511K 1% .125W F TC=0+=100 RESISTOR 511 1% .125W F TC=0+=100 RESISTOR 5.11K 1% .125W F TC=0+=100 RESISTOR 10K 1% .125W F TC=0+=100 RESISTOR 5.11K 1% .125W F TC=0+=100	28480 24546 24546 24546 24546	0757=0482 C4=1/8=70=511R=F C4=1/8=70=5111=F C4=1/8=70=1002=F C4=1/8=70=5111=F
43K11 43K12 43K13 43K14 43K15	0757-0416 0698-3440 0698-3450 0757-0399 0698-0083	7 7 9 5 8	5 6	RESISTOR 511 1% .125W F TC=0+=100 RESISTOR 196 1% .125W F TC=0+=100 RESISTOR 42.2K 1% .125W F TC=0+=100 RESISTOR 82.5 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C4=1/8=T0=511R=F C4=1/8=T0=196R=F C4=1/8=T0=4222=F C4=1/8=T0=82R5=F C4=1/8=T0=1961=F
A3K16 A3K17 A3R1R A3R19 A3K20	0698-3154 0757-0280 0757-0346 0757-0442 0757-0280	0 3 2 9 3	15	RESISTOR 4,22% 1% ,125% F TC#0+=100 RESISTOR 1K 1% ,125% F TC#0+=100 RESISTOR 10 1% ,125% F TC#0+=100 RESISTOR 10K 1% ,125% F TC#0+=100 RESISTOR 1K 1% ,125% F TC#0+=100	24546 24546 24546 24546 24546	C4-1/8-T0-4221=F C4-1/8-T0-1001=F C4-1/8-T0-10R0=F C4-1/8-T0-1002=F C4-1/8-T0-1001=F
43 2 2 1 43 2 2 2 43 2 2 3 43 2 3 4 43 2 5	0757-0438 0698-3440 0757-0442 0757-0399 0698-0083	3 7 9 5 8		RESISTOR 5.11K 1% .125W F TC=0+-100 RESISTOR 196 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 82.5 1% .125W F TC=0+-100 RESISTOR 1.96K 1% .125W F TC=0+-100	24546 24546 24546 24546 24546	C4-1/8-T0-5111=F C4-1/8-T0-196R=F C4-1/8-T0-1002=F C4-1/8-T0-28R5=F C4-1/8-T0-1961=F
43R26 43K27 43K29 43K29 43K30	0757-0198 0757-0394 0757-0394 0757-0438 0757-0280	0 0 3 3	1	RESISTOR 100 1% .5W F TC=0+=100 RESISTOR 51.1 1% .125W F TC=0+=100 RESISTOR 51.1 1% .125W F TC=0+=100 RESISTOR 5.11K 1% .125W F TC=0+=100 RESISTOR 1K 1% .125W F TC=0+=100	28480 24546 24546 24546 24546	0757-0198 C4-1/8-T0-51R1-F C4-1/8-T0-51R1-F C4-1/8-T0-5111-F C4-1/8-T0-5101-F
A 3 R 3 1	0757-0438	3		RESISTOR 5,11K 1% ,125W F TC=0+=100	24546	C4-1/8-T0-5111-F
43 V P 1	1902-3036	3	1	DIODE=ZNR 3.16V 5% DO=7 PD=.4W TC==.064%	28480	1902=3036
				A3 MISCELLANEOUS		
	0360-1514 1480-0073 4040-0748 4040-0749	7 6 3 4	11 5 1	TERMINAL-STUD SGL=PIN PRESS-MTG PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU EXTRACTOR-PC BOARD BLK POLYC EXTRACTOR-PC BOARD BRN POLYC	28480 28480 28480 28480	0360-1514 1480-0073 4040-0748 4040-0749
Δ4	86602-60003	3	1	DETECTOR AMPLIFIER ASSY	28480	86602-60003
Δ / 1 C 1 Δ / 1 C 2 Δ / 1 C / 1 Δ / 1 C / 1 Δ / 1 C / 1	0180=0116 0180=0116 0160=2207 0160=2244 0180=1743	1 1 3 8 2	1 2 1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA CAPACITOR-FXD 6.8UF+-10% 35VDC TA CAPACITOR-FXD 300PF +-5% 300VDC MICA CAPACITOR-FXD 3DF +25PF 500VDC CER CAPACITOR-FXD .1UF+-10% 35VDC TA	56289 56289 28480 28480 56289	1500685x9035B2 1500685x9035B2 0160=2207 0160=2244 1500104x9035A2
4 u C n	0160-2244	8		CAPACITOR=FXD 3PF +=.25PF 500VDC CER	28480	0160-2244
44091	1901-0050	3		DIODE-SWITCHING BOV 200MA 2NS DO+35	28480	1901-0050
∆ u × 1	0490-0916	6		RELAY-REED 14 500MA SOVDC SVDC-COIL 10VA	28480	0490=0916
4465	9140-0237 9140-0237	5		COIL-MLD 200UH 5% Q=65 .155DX.375LG=NOM COIL-MLD 200UH 5% Q=65 .155DX.375LG=NOM	28480 28480	9140=0237 9140=0237
© 11 00 € © 12 00 € © 13 00 € © 13 00 €	1853-0034 1853-0034 1854-0221 1854-0404 1853-0020	00004		TRANSISTOR PNP SI TO-18 PD=360MW TRANSISTOR PNP SI TO-18 PD=360MW TRANSISTOR-DUAL NPN PD=750MW TRANSISTOR NPN SI TO-18 PD=360MW TRANSISTOR PNP SI PD=360MW FT=150MHZ	28480 28480 28480 28480 28480	1853=0034 1853=0034 1854=0221 1854=0404 1853=0020
♥ 1 K 4 ♥ 1 K 5 ♥ 7 K 5 © 9 M 1	0698-3453 0698-3453 0757-0465 0757-0438 0698-3453	2 6 3 2	5	RESISTOR 196K 1% .125W F TC=0+=100 RESISTOR 196K 1% .125W F TC=0+=100 RESISTOR 100K 1% .125W F TC=0+=100 RESISTOR 5.11K 1% .125W F TC=0+=100 RESISTOR 196K 1% .125W F TC=0+=100	24546 24546 24546 24546	C4=1/8=T0=1963=F C4=1/8=T0=1963=F C4=1/8=T0=1003=F C4=1/8=T0=111=F C4=1/8=T0=1963=F
0 4 k 6 4 2 k 7 4 4 k P 4 4 k R P	0698-3155 0757-0438 0757-0465 0698-5844 0698-3159	1 3 6 9 5	1 1 1	RESISTOR 4.64K 1% .125W F TC*0**100 RESISTOR 5.11K 1% .125W F TC*0**100 RESISTOR 100K 1% .125W F TC*0**100 RESISTOR 4.5M 5% .25W FC TC**9*00/*1100 RESISTOR 26.1K 1% .125W F TC**0**100	24546 24546 24546 01121 24546	C4=1/8=T0=4641=F C4=1/8=T0=5111=F C4=1/8=T0=1003=F C64355 C4=1/8=T0=2612=F
AJF 1 1 AJF 1 2 AJF 1 3 AJF 1 J AJF 1 J	0698+3440 0698=3453 2100+2517 0757+0420 0698+0083	7 2 4 3 8	1	RESISTOR 196 1% .125W F TC=0+=100 RESISTOR 196K 1% .125W F TC=0+=100 RESISTOR=TRMR 50K 10% C SIDE=ADJ 1=TRN RESISTOR 750 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100	24546 24546 30983 24546 24546	C4=1/8=T0=196R=F C4=1/8=T0=1963=F ET50X503 C4=1/8=T0=751=F C4=1/8=T0=1961=F

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R16 A4R17*	0698-0083 0698-3442	8 9	1	RESISTOR 1.96K 1% .125W F TC=0+=100 RESISTOR 237 1% .125W F TC=0+=100 *FACTORY SELECTED PART	24546	C4=1/8=T0=1961=F C4=1/8=T0=2378=F
Auf. 18 Auf. 19	0757-0280 0698-3447	3 4	2	RESISTOR 1K 1% .125W F TC=0+-100 RESISTOR 422 1% .125W F TC=0+-100	24546 24546	C4-1/8-T0-1001-F C4-1/8-T0-422R-F
A 4 R 2 O A 4 R 2 1 A 4 R 2 2 A 4 R 2 3 A 4 R 2 4	0698-0082 0698-3447 0698-3157 0698-3455 0757-0439	7 4 3 4 4	1 0 1 1 3	RESISTOR 464 1% ,125W F TC=0+=100 RESISTOR 422 1% ,125W F TC=0+=100 RESISTOR 19,6K 1% ,125W F TC=0+=100 RESISTOR 261K 1% ,125W F TC=0+=100 RESISTOR 6,81K 1% ,125W F TC=0+=100	24546 24546 24546 24546 24546	C4-1/8-T0-4640-F C4-1/8-T0-4228-F C4-1/8-T0-1962-F C4-1/8-T0-2613-F C4-1/8-T0-6811-F
A4R25	0698=0082 2100=2489	7 9	1	RESISTOR 464 1% .125W F TC=0+=100 RESISTOR=TRMR 5K 10% C SIDE=ADJ 1=TRN	24546 30983	C4-1/8-T0-4640-F ET50×502
A4S1	3101-0973	5	1	SWITCH-SL OPDI-NS MINTR .54 125VAC/DC PC	28480	3101-0975
1910	0360=1514 0360=1514	7 7		TERMINAL-STUD SGL-PIN PRESS-MTG TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360=1514 0360=1514
4401	1826-0013	8	2	IC 741 OP AMP TO-99	06665	SSS741CJ
	4040=0748 1480=0073 4040=0751	3 6 8	1	A4 MISCELLANEOUS EXTRACTOR-PC BOARD BLK POLYC PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU EXTRACTOR-PC BOARD ORN POLYC	28480 28480 28480	4040=0748 1480=0073 4040=0751
A5	5086-7049	8	1	MODULATOR ASSY	28480	5086=7049
A 6	5086-7119	3	1	1-1300 MHZ AMPLIFIER ASSEMBLY	28480	5086-7119
Δ7	86602-60044	5	1	MIXER ASSY (EXCEPT OPTION 002)	28480	86602-60044
47J1 47J2 47J3	85002-20022 85002-20022	5 5		CONNECTOR BULKHEAD CONNECTOR BULKHEAD CONNECTOR BULKHEAD	28480 28480 28480	\$\$002~\$0048 \$\$005~\$0048
	0360=0124 5001=0002 86602=00003 86602=20026 86602=20029	3 1 7 6 9 0 5	5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	A7 MISCELLANEOUS CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND COVER, FILTER COVER, MIXER, SMALL BUSHING SUPPRESSOR COVER, MIXER, LARGE HOUSING, MIXER	28480 28480 28480 28480 28480 28480	0360=0124 5001=0002 86602=00003 86602=20026 86602=20029 86603=00005 86603=20024
A 7 A 1	86602=20009	5		BALUN MIXER ASSEMBLY	28480	86602-20009
A7A2	86602-60008	8		BALANCE MIXER ASSY	28480	86602=60008
4742CR1	5080-0271	5		DIODE QUAD	28480	5080=0271
A7A3	5086=7066	9		LOW PASS FILTER ASSY, 1.45 GMZ	28480	5086=7066
A7A4	86003-20023	4		TRANSITION ASSEMBLY	28480	86603-20023
A7A5	86605=50044	8	1	TRANSITION ASSEMBLY	28480	86602-20044

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
Δ 7	86603=60023	8	1	MIXER ASSY (OPTION 002 ONLY)	28480	86603-60023
A 7 C 1	0160-4082	6	1	CAPACITOR-FOTHRU 1000PF 20% 200V CER	28480	0160-4082
△ 7 J 1 △ 7 J 2 △ 7 J 3	\$2002-20098 \$2002-20098 \$2005-20098	5 5	6	CONNECTOR, BULKHEAD CONNECTOR, BULKHEAD CONNECTOR, BULKHEAD	28480 28480 28480	86602=20022 86002=20022 86602=2022
A 7 L 1	9100=1666	9	1	COIL-MLD 3.6MH 5% Q=70 .215Dx.56LG-NOM	28480	9100=1666
	0340=0044 0360=0124 5001=0002 86602=00003 86602=20026	4 3 1 7 6	S	TERMINAL-STUD DBL-TUR PRESS-MTG CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND COVER, FILTER COVER, MIXER, SMALL BUSHING	28480 28480 28480 28480	0340=0044 0360=0124 5001=0002 86602=00003 86602=20026
	86602=20029 86603=00005 86603=20024	0 5		SUPPRESSOR COVER, MIXER, LARGE HOUSING, MIXER	28480 28480 28480	86602=20029 86603=00005 86603=20024
27A1	86602=20009	5	2	BALUN MIXER ASSY	28480	86602=20009
742	86602=60008	8	5	BALANCE MIXER ASSY	28480	86602-60008
174>CR1	5080-0271	5	5	DIODE QUAD	28480	5080-0271
λ 7 Δ 5	5086=7066	9	5	LOW PASS FILTER ASSY, 1.45 GHZ	28480	5086=7066
7 A u	86603=20023	4	5	TRANSITION ASSEMBLY	28480	86603-20023
1745	86603=60010	3	1	LOW PASS FILTER ASSY, 50 MHZ	28480	86603=60010
4745C1 4745C2 4745C3 4745C4 4745C5	0160-4303 0160-4305 0160-4308 0160-4247 0160-4303	46954	2 1 1 1 13	CAPACITOR=FXD .027UF +=10% 50VDC CER CAPACITOR=FXD 47PF +=10% 100VDC CER CAPACITOR=FXD 33PF +=10% 100VDC CER CAPACITOR=FXD .047UF +=20% 100VDC CER CAPACITOR=FXD .027UF +=10% 50VDC CER	26654 28480 16546 28480 26654	3BX50S273K 0160=4305 N100BC330K(PD/AG) 0160-4247 3BX50S273K
74500	0160=0575	4	5	CAPACITOR-FXD .047UF +=20% 50VDC CER	28480	0160-0575
745CR1	1901=0639 1901=0639	4 4	S	DIODE=PIN 110V DIODE=PIN 110V	28480 28480	5082=3080 5082=3080
174561	86603=80001 86603=80001	4	5	INDUCTOR, TOROID INDUCTOR, TOROID	28480 28480	86603-80001 86603-80001
4745P1 4745P2 4745R3	0698-7222 0698-7222 0698-7229	1 8	3	RESISTOR 261 1% .05W F TC=0+=100 RESISTOR 261 1% .05W F TC=0+=100 RESISTOR 511 1% .05W F TC=0+=100	24546 24546 24546	C3=1/8=T0=261R=G C3=1/8=T0=261R=G C3=1/8=T0=511R=G
4 A	86603=67003 86603=67001	8 6	1	4 GHZ AMPLIFIER ASSY(EXCEPT OPT 002) 4 GHZ AMPLIFIER ASSY(OPTION 002 ONLY)	58480 58480	86603=67003 86603=67001
10+	86601-60129	3	1	ATTENUATOR DRIVER ASSEMBLY	28480	86601=60129
49C1 49C2 49C3	0160=0127 0160=0127 0160=0127 0160=0127	5 5 5 5 5 5 5	7	(EXCEPT OPTION 001) CAPACITOR=FXD 1UF +=20% 25VDC CER	28480 28480 28480 28480	0160=0127 0160=0127 0160=0127 0160=0127
70051 70051 70051	1480-0073 1480-0073 4040-0752 4040-0752	0000	5	PIN=ROLL .062=IN=DIA .25=IN=LG BE=CU PIN=ROLL .062=IN=DIA .25=IN=LG BE=CU EXTRACTOR=PC BOARD YEL POLYC EXTRACTOR=PC BOARD YEL POLYC	28480 28480 28480 28480	1480=0073 1480=0073 4040=0752 4040=0752
1961 1967 1976	1853=0213 1854=0361 1853=0213 1854=0361 1854=0071	7 8 7 8 7	10	TRANSISTOR PNP 2N4236 SI TO=5 PD=1W TRANSISTOR NPN 2N4239 SI TO=5 PD=800MW TRANSISTOR PNP 2N4236 SI TO=5 PD=1W TRANSISTOR NPN 2N4239 SI TO=5 PD=800MW TRANSISTOR NPN SI PD=300MW FT#200MHZ	04713 04713 04713 04713 28480	2N4236 2N4239 2N4236 2N4239 1854-0071
49.45 49.47 49.49 49.41	1853-0020 1854-0071 1853-0020 1853-0213 1854-0361	4 7 4 7 8		TRANSISTOR PNP SI PD#300MW FT#150MHZ TRANSISTOR NPN SI PD#300MW FT#200MHZ TRANSISTOR PNP SI PD#300MW FT#150MHZ TRANSISTOR PNP 2N4236 SI TO=5 PD#1W TRANSISTOR NPN 2N4236 SI TO=5 PD#800MW	28480 28480 28480 04713	1853-0020 1854-0071 1853-0020 2N4235
29511 29517 29513 19614 2016	1853-0213 1854-0361 1854-0071 1853-0020 1854-0071	7 8 7 4 7		TRANSISTOR PNP 204236 SI TO=5 PD=1W TRANSISTOR NPN 204239 SI TO=5 PD=800MW TRANSISTOR NPN SI PD=300MW FT=200MHZ TRANSISTOR NPN SI PD=300MW FT=150MHZ TRANSISTOR NPN SI PD=300MW FT=150MHZ	04713 04713 28480 28480 28480	2N4236 2N4239 1854=0071 1853=0020 1854=0071

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9616	1853=0020	4		TRANSISTOR PNP SI PD=300Mw FT=150MHZ	28480	1853=0020
A9%1 A0R2 A9R3 A9R4	0757-0280 0757-0280 0757-0280 0757-0280 0757-0159	3 3 3 5	8	RESISTOR 1K 1% .125W F TC=0+-100 RESISTOR 1K 1% .5W F TC=0+-100	24546 24546 24546 24546 28480	C4-1/8-T0-1001-F C4-1/8-T0-1001-F C4-1/8-T0-1001-F C4-1/8-T0-1001-F 0757-0159
4986 + 4987 + 4988 + 49810 + 4	0698-3440 0757-0159 0757-0159 0698-3440 0757-0159	7 5 7 5		RESISTOR 196 1% ,125% F TC=0+=100 RESISTOR 1% 1% ,5% F TC=0+=100 RESISTOR 1% 1% ,5% F TC=0+=100 RESISTOR 196 1% ,125% F TC=0+=100 RESISTOR 1% 1% ,5% F TC=0+=100	24546 28480 28480 24546 28480	C4-1/8-T0-196R-F 0757-0159 0757-0159 C4-1/8-T0-196R-F 0757-0159
AGR11 AGR12 AGR13 AGR14 AGR15	0757-0159 0698-3440 0757-0159 0757-0159 0757-0401	5 7 5 5		RESISTOR 1K 1% 5W F TC=0+=100 RESISTOR 196 1% .125W F TC=0+=100 RESISTOR 1K 1% .5W F TC=0+=100 RESISTOR 1K 1% .5W F TC=0+=100 RESISTOR 100 1% .125W F TC=0+=100	28480 24546 28480 28480 24546	0757=0159 C4=1/8=T0=196R=F 0757=0159 0757=0159 C4=1/8=T0=101=F
AGR16 AGR18 AGR18 AGR19 AGR20	0757-0159 0698-0082 0698-0082 0698-0082 0698-0082	5 7 7 7		RESISTOR 1K 1% ,5W F TC=0+-100 RESISTOR 464 1% ,125W F TC=0+-100	24546 24546 24546 24546	0757-0159 C4-1/8-T0-4040-F C4-1/8-T0-4040-F C4-1/8-T0-4640-F C4-1/8-T0-4640-F C4-1/8-T0-4640-F
49821 49822 49823 49824 49825	0698-0082 0698-0082 0698-0082 0698-0082 0683-0335	7 7 7 7 7 2	1	RESISTOR 464 1% .125W F TC=0+=100 RESISTOR 3.3 5% .25W FC TC=400/+500	24546 24546 24546 24546 01121	C4=1/8=T0=4640=F C4=1/8=T0=4640=F C4=1/8=T0=4640=F C4=1/8=T0=4640=F C833G5
49VR1 49VR2 49VR3 49VRU	1902-3002 1902-3002 1902-3002 1902-3002	3 3 3 3	4	DIODE-ZNR 2,37V 5% D0-7 PD=,4W TC=-,074%	28480 28480 28480 28480	1902-3002 1902-3002

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
10	86602-60006	6	1	REFERENCE ASSY	28480	86602∞60006
1001	6000500000		1	NOT ASSIGNED	20400	66602#60006
71005	0180=0291	3	5	CAPACITOR-FXD 1UF+=10% 35VDC TA	56289	150D105x9035A2
110K1 110K2 110K4 110K4	0490=0916 0490=0916 0490=0916 0490=0916 0490=0916	00000		RELAY-REED 1A 500MA 50VDC 5VDC-COIL 10VA	28480 28480 28480 28480 28480	0490=0916 0490=0916 0490=0916 0490=0916
Aloks	0490=0916	6		RELAY-REED 14 500MA 50VDC SVDC-COIL 10VA	28480	0490=0916
41001 41002 41002 41004 41004	1853=0020 1853=0020 1853=0020 1853=0020 1853=0020	4 4 4 4 4		TRANSISTOR PNP SI PDB300MW FTE150MHZ	28480 28480 28480 28480	1853=0020 1853=0020 1853=0020 1853=0020 1853=0020
41006 41007 41009 41009 410010	1853-0020 1853-0020 1853-0020 1853-0020 1854-0404	9 4 4 9 0		TRANSISTOR PNP SI PD=300MW FT=150MHZ TRANSISTOR NPN SI TD=18 PD=360MM	28480 28480 28480 28480	1853-0020 1853-0020 1853-0020 1853-0020 1854-0404
410011	1855-0082	2	1	TRANSISTOR J-FET P-CHAN D-MODE SI	28480	1855=0082
A 1 0 P 1 A 1 0 P 2 A 1 0 P 3 A 1 0 P 3 A 1 0 P 3 A 1 0 P 5	0757-0279 2100-2517 0757-0280 0757-0817 2100-2633	0 4 3 2 5	1 1 3	RESISTOR 3,16K 1% ,125W F TC=0+=100 RESISTOR=TRMR 50K 10% C SIDE=ADJ 1=TRN RESISTOR 1K 1% ,125W F TC=0+=100 RESISTOR 750 1% ,5W F TC=0+=100 RESISTOR=TRMR 1K 10% C SIDE=ADJ 1=TRN	24546 30983 24546 28480 30983	C4-1/8-T0-3161-F ET50x503 C4-1/8-T0-1001-F 0757-0817 ET50x102
41096 41097 41098 41099 41094	0757-0443 2100-2633 0757-0416 0757-0260 0698-3260	0 5 7 3	1	RESISTOR 11% 1% ,125W F TC=0+=100 RESISTOR=TRMR 1% 10% C SIDE=4DJ 1=TRN RESISTOR 511 1% ,125W F TC=0+=100 RESISTOR 1% 1% ,125W F TC=0+=100 RESISTOR 464% 1% ,125W F TC=0+=100	24546 30983 24546 24546 28480	C4-1/8-T0-1102=F ET50X102 C4-1/8-T0-511R=F C4-1/8-T0-1001=F 0698-3260
410-711 410-712 410-713 410-713 410-715	0698-3260 0698-3453 0757-0439 0683-1065 0757-0280	9 2 4 7 3	1	RESISTOR 464K 1% .125W F TC=0+=100 RESISTOR 196K 1% .125W F TC=0+=100 RESISTOR 6,81K 1% .125W F TC=0+=100 RESISTOR 10M 5% .25W FC TC==000/+1100 RESISTOR 1 K 1% .125W F TC=0+=100	26480 24546 24546 01121 24546	0698-3260 C4-1/8-T0-1963-F C4-1/8-T0-6811-F C81065 C4-1/8-T0-1001-F
410×16 410×17 410×18 410×19 410×20	0698-3450 0757-0280 0698-0083 0698-0083 0698-0083	9 3 8 8 8		RESISTOR 42.2K 1% .125W F TC=0+=100 RESISTOR 1K 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C4-1/8-T0-4222=F C4-1/8-T0-1001=F C4-1/8-T0-1961=F C4-1/8-T0-1961=F C4-1/8-T0-1961=F
410P21 410~22 410P23 410P24 410P25	0698-4406 0698-4462 0698-4406 0698-0083 0698-0083	7 9 7 8 8	2	RESISTOR 115 1% +125W F TC=0+=100 RESISTOR 17,4K 1% +125W F TC=0+=100 RESISTOR 115 1% +125W F TC=0+=100 RESISTOR 1,96K 1% +125W F TC=0+=100 RESISTOR 1,96K 1% +125W F TC=0+=100	24546 03888 24546 24546 24546	C4-1/8-T0-115R-F PME55-1/8-T0-1742-F C4-1/8-T0-115R-F C4-1/8-T0-1961-F C4-1/8-T0-1961-F
410926 410927 410928 410929 410930	0698-3466 0698-3498 0698-3486 0698-0083 0698-0083	1 8 8	1	RESISTOR 232 1% .125W F TC=0+=100 RESISTOR 8.66K 1% .125W F TC=0+=100 RESISTOR 232 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C4-1/8-T0-232R=F C4-1/8-T0-866R=F C4-1/8-T0-232R=F C4-1/8-T0-1961=F C4-1/8-T0-1961=F
410R31 410R32 410R33 410R35	0698-3510 0698-3154 0698-3510 0698-0083 0698-0083	8 8 0 0 0	S	RESISTOR 453 1% .125W F TC=0+=100 RESISTOR 4.22K 1% .125W F TC=0+=100 RESISTOR 453 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100	24546 24546 24546 24546	C4-1/8-T0-453R=F C4-1/8-T0-4221=F C4-1/8-T0-453R=F C4-1/8-T0-1961=F C4-1/8-T0-1961=F
A10836 A10237 A10238 A10238 A10238 A10240	0698-3495 0698-4430 0698-3495 0757-0280 0757-0442	2 7 2 3 9	1	RESISTOR 866 1% .125W F TC=0+=100 RESISTOR 1.91K 1% .125W F TC=0+=100 RESISTOR 866 1% .125W F TC=0+=100 RESISTOR 1K 1% .125W F TC=0+=100 RESISTOR 1K 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C4-1/8-T0-800R=F C4-1/8-T0-1911=F C4-1/8-T0-800R=F C4-1/8-T0-1001=F C4-1/8-T0-1002=F
410941	0757-0442	9		RESISTOR 10K 1% ,125W F TC=0+=100	24546	C4-1/8-T0-1002-F
11091	1826=0081	0	1	IC 318 OP AMP TO=99	27014	LM318H
417.81	1902-0041	4	3	DIODE-ZNR 5,11V 5% DO-7 PD=,4W TC=-,009%	28480	1902-0041
	4040=0753 1480=0073	0 6	5	A10 MISCELLANEOUS EXTRACTOR-PC HOARD GRN POLYC PIN-ROLL ,062-IN-DIA ,25-IN-LG HE-CU	28480 28480	4040=0753 1480=0073

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A11	86603-60029	4	1	LOGIC ASSY	28480	86603-60029
A 1 1 C 1	0180-2206	4	1	CAPACITOR=FXD 60UF+=10% 6VDC TA	56289	150D606x900682
A11L1	9140=0105	3		COIL-MLD 8.2UH 10% Q#50 .155DX.375LG=NOM	28480	9140=0105
A1101 A1102 A1103 A1104 A1105	1820-0508 1820-0077 1820-0069 1820-0305 1820-0054	42295	1 1 2 5	IC RGTR TTL BFR 10=BIT IC FF TTL D=TYPE PDS=EDGE=TRIG CLEAR IC GATE TTL NAND DUAL 4=INP IC ADDR TTL FULL ADDER 4=BIT IC GATE TTL NAND QUAD 2=INP	18324 01295 01295 01295 01295	N8202N SN747UN SN742ON SN7483AN SN740ON
A11U6 A11U7 A11U8 A11U8 A11U9 A11U10	1820-0054 1820-0305 1820-0174 1820-0054	59055	ŝ	IC GATE TTL NAND GUAD 2=INP IC ADDR TTL FULL ADDER 4=8IT IC INV TTL HEX IC GATE TTL NAND GUAD 2=INP IC GATE TTL NAND GUAD 2=INP	01295 01295 01295 01295 01295	\$N7400N \$N7463AN \$N7404N \$N7400N \$N7400N
				A11 MISCELLANEOUS		
	4040=0754 1480=0073 86603=00007 0380=0803	1 6 2 7	1 4	EXTRACTOR-PC BOARD BLU POLYC PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU INSULATOR SPACER-RND .094-IN-LG .091-IN-ID	28480 28480 28480 28480	4040=0754 1480=0073 86603=00007 0380=0803
△ 1 ∂	86602-60038	4	1	LOGIC MOTHER BOARD ASSY	28480	86602=60038
W15C5	0160=2055 0160=2055	9 9	3	CAPACITOR-FXD .01UF +80=20% 100VDC CER CAPACITOR-FXD .01UF +80=20% 100VDC CER	28480 28480	0160=2055 0160=2055
A12L1 A12L2	9140=0144 9140=0144	0 0	2	COIL-MLD 4.7UH 10% Q=45 .095DX.25LG-NOM COIL-MLD 4.7UH 10% Q=45 .095DX.25LG-NOM	28480 28480	9140=0144
AISXA9	1251-1626	2		CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251+1626
A12XA10 A12XA11	1251-2034 1251-2035	8	1 1	CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	28480 28480	1251-2034 1251-2035
A 1 3 A 1 3	86603-60043 86601-60109	2 9	1	ATTENUATOR ASSY(EXCEPT OPTION 001) RESTORED 86603-60043, REQUIRES EXCHANGE	28480 28480	8 6 6 0 3 = 6 0 0 4 3 8 6 6 0 1 = 6 0 1 0 9
A13J1 A13J2				NSR NSR		
414	86603-60020	5	1	WIRING MARNESS, MAIN(INCLUDES P5, P7,	28480	86603=60020
	1251-3087	3	30	P13, P14, AND XAZ1) CONTACT-CONN U/W-RECT FEM CRP	28480	1251=3087
A15	86602-60035	1	1	20 MHZ AMPLIFIER ASSY	28480	86602=60035
A 1 5 C 1	0160-2437	1	7	CAPACITOR=FDTHRU 5000PF +80 =20% 200V	28480	0160-2437
A15J1	1250=1194	7	3	CONNECTOR-RF SM-SLO M SGL-HOLE-FR 50-OHM	28480	1250-1194
A15J2	1250-1194	7		NSR CONNECTOR-RF SM-SLD M SGL-MOLE-FR 50-0HM NSR	28480	1250-1194
A16 †	86603-60041	0	1	BOARD ASSEMBLY, PHASE MODULATOR DRIVER	28480	86603-60041
A1001 A1002 A1003 A1004 A1005	0180=0228 0100=0575 0160=0127 0160=0575 0160=0575	0 4 N 4 4	1	CAPACITOR=FXD 22UF+=10X 15VDC TA CAPACITOR=FXD .047UF +=20X 50VDC CER CAPACITOR=FXD 1UF +=20X 25VDC CER CAPACITOR=FXD .047UF +=20X 50VDC CER CAPACITOR=FXD .047UF +=20X 50VDC CER	56289 28480 28480 28480 28480	1500226×901582 0160=0575 0160=0127 0160=0575 0160=0575
A1006 A1007 A1008 A1009	0180=0374 0121=0494 0160=4084 0160=0575	3 4 8 4	1 1 1	CAPACITOR=FXD 10UF+=10% 20VDC TA CAPACITOR=V TRMR=CER 2,5=6FF 250V PC=MTG CAPACITOR=FXD ,1UF +=20% 50VDC CER CAPACITOR=FXD ,047UF +=20% 50VDC CER	56289 52763 28480 28480	1500106x902002 7-3 TRIKO-13 0160-4084 0160-0575
A10CR1 A10CR2 A10CR3 A10CR4 A10CR5	1901=0179 1901=0179 1901=0033 1901=0033 1901=0033	7 7 2 2 2 2	10	DIODE-SWITCHING 15V 50MA 750PS DO-7 DIODE-SWITCHING 15V 50MA 750PS DO-7 DIODE-GEN PRP 180V 200MA DO-7 DIODE-GEN PRP 180V 200MA DO-7 DIODE-GEN PRP 180V 200MA DO-7	28480 28480 28480 28480 28480	1901=0179 1901=0179 1901=0033 1901=0033 1901=0033
A16CR6 A16CR7 A16CR8 A16CR9	1901-0539 1901-0033 1901-0033 1901-0033	3 2 2	1	DIODE-SCHOTTKY DIODE-GEN PRP 180V 200MA DO-7 DIODE-GEN PRP 180V 200MA DO-7 DIODE-GEN PRP 180V 200MA DO-7	28480 28480 28480 28480	1901=0539 1901=0033 1901=0033 1901=0033
A16E1	0410=0184	5	1	OVENSCRYSTAL-COMPONENT & USE/TO-18	73803	5871=2
A10J1 A10J2	1250=1377	8	2	CONNECTOR-RF SM8 FEM PC 50-0HM CONNECTOR-RF SM8 FEM PC 50-0HM	28480 28480	1250=1377 1250=1377

Table 6-3. Replaceable Parts

Reference HP Part C Ott. Description Mfr Mfr Part Number								
Designation Designation	Number Number	D	Qty	Description	Code	Mfr Part Number		
A16L1	9140-0158	6		COIL-MLD 1UH 10% Q=32 .095DX.25LG-NOM	28480	9140=0158		
A1601 A1602 A1603 A1604 A1604	1853-0075 1854-0295 1853-0075 1855-0327 1854-0457	9 7 9 8 3	1 1	TRANSISTOR-DUAL PNP PD=400MW TRANSISTOR-DUAL NPN PD=400MW TRANSISTOR-DUAL PNP PD=400MW TRANSISTOR J=FET 2N4416 N=CHAN D=MODE TRANSISTOR=DUAL NPN PD=400MW	28480 28480 28480 01295 28480	1853=0075 1854=0295 1853=0075 2N4416 1854=0457		
A1606 A1607 A1606 A1609 A16010	1853-0352 1854-0013 1853-0012 1853-0451 1854-0023	57 4 5 9	1 2 1 2	TRANSISTOR PNP SI TO-92 PD=350MW FT=1GHZ TRANSISTOR NPN 2N2218A SI TO-5 PD=800MW TRANSISTOR PNP 2N2904A SI TO-39 PD=600MW TRANSISTOR PNP 2N3799 SI TO-18 PD=360MW TRANSISTOR NPN SI TO-18 PD=360MW	28480 04713 01295 01295 28480	1853-0352 2N2218A 2N2904A 2N3799 1854-0023		
A1681 A1682 A1683 A1684 A1685 **	2100-3095 2100-3095 0698-7236 0698-7241 0698-7236	5 7 4 7	2 8 1	RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN RESISTOR IK 1% 05% F TC=00+=100 RESISTOR 1, 02K 1% 05% F TC=00+=100 RESISTOR 1K 1% 05% F TC=00+=100	02111 02111 24546 28480 24546	43P201 43P201 C3-1/8-T0-1001-G 0698-7241 C3-1/8-T0-1001-G		
A10R6 A10R7 A10R8 A10R9 A10R10	0698=7234 0698=7236 0698=7226 0698=7236 0698=7216	5 7 5 7 3	1 1 1	RESISTOR 825 1% ,05W F TC=0+=100 RESISTOR 1K 1% ,05W F TC=0+=100 RESISTOR 383 1% ,05W F TC=0+=100 RESISTOR 1K 1% ,05W F TC=0+=100 RESISTOR 1K 1% ,05W F TC=0+=100 RESISTOR 1K 1% ,05W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T0-825R=G C3-1/8-T0-1001-G C3-1/8-T0-383R=G C3-1/8-T0-1001-G C3-1/8-T0-1047R-G		
A10R11 A10R12 A10R13 A10R14 A10R15	0698=7260 0698=7217 0698=7212 0698=7260 0698=0083	7 4 9 7 8	10 2 7	RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 162 1% .05W F TC=0+=100 RESISTOR 100 1% .05W F TC=0+=100 RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 1,96K 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T0-1002-G C3-1/8-T0-102R-G C3-1/8-T0-100R-G C3-1/8-T0-1002-G C4-1/8-T0-1096-F		
A16R16 A16R17 A16R18 A16R19 A16R20	0698=7200 0698=7221 0698=7260 0698=7200 0698=7221	5 0 7 5 0	3	RESISTOR 31.6 1% .05W F TC=0+=100 RESISTOR 237 1% .05W F TC=0+=100 RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 31.6 1% .05W F TC=0+=100 RESISTOR 237 1% .05W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T00-31R6-G C3-1/8-T0-237R-G C3-1/8-T0-1002-G C3-1/8-T00-31R0-G C3-1/8-T0-237R-G		
A16R21 A16R22 A16R23 A16R24 A16R25	0698=7260 0698=7217 0698=7212 0698=7209 0698=0083	7 4 9 4 8	1	RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 162 1% .05W F TC=0+=100 RESISTOR 100 1% .05W F TC=0+=100 RESISTOR 75 1% .05W F TC=0+=100 RESISTOR 1.96K 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T0-1002-G C3-1/8-T0-162R-G C3-1/8-T0-100R-G C3-1/8-T00-75R0-G C4-1/8-T0-1961-F		
A16R26 A16R27 A16R28 A16R29 A16R30	0698=7213 2100=2633 0698=0083 0698=7213 0698=7219	0 5 8 0 6	3	RESISTOR 110 1% .05W F TC=0+=100 RESISTOR=TRMR 1K 10% C SIDE=ADJ 1=TRN RESISTOR 1.96K 1% .125W F TC=0+=100 RESISTOR 110 1% .05W F TC=0+=100 RESISTOR 196 1% .05W F TC=0+=100	24546 30983 24546 24546 24546	C3-1/8-T0-110R-G ET50X102 C4-1/8-T0-1961-F C3-1/8-T0-110R-G C3-1/8-T0-196R-G		
A16R31 A16R32 A16R33 A16R34 A16P35	0698=7236 0698=7248 0698=7219 0698=7243 0757=0418	7 1 6 6 9	3 4 1	RESISTOR 1K 1% .05W F TC=0+=100 RESISTOR 3.16K 1% .05W F TC=0+=100 RESISTOR 19-6 1% .05W F TC=0+=100 RESISTOR 1.96K 1% .05W F TC=0+=100 RESISTOR 619 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T0=1001=G C3-1/8-T0-3161=G C3-1/8-T0-196R=G C3-1/8-T0-1961=G C4-1/8-T0-619R=F		
A 1 0 R 3 0 A 1 0 R 3 7 A 1 0 R 3 8 A 1 0 R 3 9 A 1 0 R 4 0	2100-3123 0757-0421 0698-7213 0698-7233 0698-7202	0 4 0 4 7	1 1 1	RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN RESISTOR 825 1% .125W F TC=0+-100 RESISTOR 110 1% .05W F TC=0+-100 RESISTOR 750 1% .05W F TC=0+-100 RESISTOR 38.3 1% .05W F TC=0+-100	02111 24546 24546 24546 24546	43P501 C4-1/8-T0-82SR-F C3-1/8-T0-110R-G C3-1/8-T0-750R-G C3-1/8-T00-38R3-G		
A16R41 A16R42 A16R43 A16R44 A16R45	0698=7212 0757=0280 0698=7212 0698=7236 0698=0085	9 3 9 7 0	i	RESISTOR 100 1% .05W F TC=0+=100 RESISTOR 1K 1% .125W F TC=0+=100 RESISTOR 100 1% .05W F TC=0+=100 RESISTOR 1K 1% .05W F TC=0+=100 RESISTOR 2.61K 1% .125W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T0-100R=G C4-1/8-T0-1001-F C3-1/8-T0-100R-G C3-1/8-T0-1001-G C4-1/8-T0-2011-F		
A 1 6 R U 6 A 1 6 R U 7 A 1 6 R U 8 A 1 6 R U 9 A 1 6 R 5 0	0698-7195 0698-7188 0698-7188 0698-7236 0698-7248	7 8 8 7	5	RESISTOR 19.6 1% .05W F TC=0+=100 RESISTOR 10 1% .05W F TC=0+=100 RESISTOR 10 1% .05W F TC=0+=100 RESISTOR 1K 1% .05W F TC=0+=100 RESISTOR 3.16K 1% .05W F TC=0+=100	24546 24546 24546 24546 24546	C3=1/8=T00=19R6=G C3=1/8=T00=10R=G C3=1/8=T00=10R=G C3=1/8=T0=1001=G C3=1/8=T0=3161=G		
A16851	0698-7195	7		RESISTOR 19.6 1% .05W F TC=0+=100	24546	C3-1/8-T00-19R6-G		
A16RT1 A16TP1	0839=0004	3	1	THERMISTOR BEAD 2K-OHM TC==3.4%/C-DEG CONNECTOR=SGL CONT PIN .04-IN-BSC-SZ RND	28480	0839=0004		
A16TP2	0360-0124	3		CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360=0124		
A16U1	1858-0032	8	1	TRANSISTOR ARRAY	01928	CA3146E		
A16VR1	1902-0554 1902-0579	3	1 1	DIODE=ZNR 10V 5% DO=15 PD=1W TC=+,06% DIODE=ZNR 5,11V 5% DO=15 PD=1W TC=-,009%	28480 28480	1902-0554 1902-0579		
	4040-0748 1480-0073 4040-0750 1480-0073	3 6 7 6	1	A16 MISCELLANEOUS EXTRACTOR-PC BOARD BLK POLYC PIN-ROLL ,062-IN-DIA ,25-IN-LG BE-CU EXTRACTOR-PC BOARD RED POLYC PIN-ROLL ,062-IN-DIA ,25-IN-LG BE-CU	28480 28480 28480	4040=0748 1480=0073 4040=0750 1480=0073		

Table 6-3. Replaceable Parts

Reference HP Part Number				Mfr Code	Mfr Part Number
A17 86603-6004	2 1	1	PHASE MODULATOR ASSEMBLY (OPTION 602 ONLY)	28480	86603-60042
A17C1 A17C2 A17C3 A17C3 A17C4 O160-4304 O160-4304	5 5 5 5	4	CAPACITOR=FXD 10PF +=10% 100VDC CER	28480 28480 28480 28480	0160-4304 0160-4304 0160-4304 0160-4304
A17CR1T 0122-0074 A17CR2T 0122-0074	8	5	DIODE-VVC .7PF 10% CO/C25-MINE4 BVRE40V DIODE-VVC .7PF 10% CO/C25-MINE4 BVRE40V	96341 96341	MA45644
A17J1 1250=1194	7		CONNECTOR-RF SM-SLD M SGL-HOLE-FR 50-OHM	28480	1250-1194
A17P1 1250=0563 A17P2 1250=0563	5 5	5	CONNECTOR-RF SMA M 4-HOLE-FLG-FR 50-OHM CONNECTOR-RF SMA M 4-HOLE-FLG-FR 50-OHM	28480 28480	1250=0563 1250=0563
			A17 MISCELLANEOUS		
86603-00004 86603-2001		1 1	COVER, PHASE MODULATOR HOUSING HOUSING, PHASE MODULATOR	28480 28480	86603=20011
A18 0955-0045	8	1	CIRCULATOR ASSY (OPTION OOZ ONLY)	28480	0955-0045
A19 0960=0426	0	1	ISOLATOR ASSY, 3.9-4.1GHZ (OPTION 002 ONLY	28480	0960=0426
A20 86603-60009	0	1	POWER SUPPLY ASSY	28480	86603-60009
A20C1 0180=1704 A20C2 0100=4247 A20C3 0160=3878 A20C4 0160=0174 A20C5 0180=0291	5 6 9 3	1 12 1 1	CAPACITOR=FXD 47UF++10X 6VDC TA CAPACITOR=FXD .047UF ++20X 100VDC CER CAPACITOR=FXD 1000PF ++20X 100VDC CER CAPACITOR=FXD .47UF ++80-20X 25VDC CER CAPACITOR=FXD 1UF++10X 35VDC TA	56289 28480 28480 28480 56289	1500476×900682 0160=4247 0160=3878 0160=0174 1500105×9035A2
A20CR1 1901-0033 A20CR2 1901-0033	5		DIODE=GEN PRP 180V 200MA DO=7 DIODE=GEN PRP 180V 200MA DO=7	28480 28480	1901=0033 1901=0033
A 2001 1853=0012 A 2002 1854=0071 A 2003 1854=0071 A 2004 1854=0071 A 2005 1854=0071	4 7 7 7 7		TRANSISTOR PNP 2N2904A SI TO-39 PD=600MW TRANSISTOR NPN SI PD=300MW FT=200MHZ	01295 28480 28480 28480 28480	2N2904A 1854=0071 1854=0071 1854=0071 1854=0071
A2006 1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A20R1 0698=7260 A20R2 0698=7243 A20R3 0698=7243 A20R4 0698=7243 A20R5 0698=7267	7 6 7 6 4	2	RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 1.96K 1% .05W F TC=0+=100 RESISTOR 1K 1% .05W F TC=0+=100 RESISTOR 1.96K 1% .05W F TC=0+=100 RESISTOR 1.96K 1% .05W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T0-1002-G C3-1/8-T0-1961-G C3-1/8-T0-1001-G C3-1/8-T0-1961-G C3-1/8-T0-1962-G
A20R6 0698=7200 A20R7 2100=2413 A20R8 0698=7242 A20R9 0698=7212 A20R10 0698=7212	5 9 8 9 9	1 1	RESISTOR 31.6 1% .05W F TC=0+=100 RESISTOR=TRMR 200 10% C SIDE=ADJ 1=TRN RESISTOR 2.37K 1% .05W F TC=0+=100 RESISTOR 100 1% .05W F TC=0+=100 RESISTOR 100 1% .05W F TC=0+=100	24546 30983 24546 24546 24546	C3=1/8=T00=31R6=G ET50X201 C3=1/8=T0=2371=G C3=1/8=T0=100R=G C3=1/8=T0=100R=G
A20R11 0698-7212 A20R12 0698-3443 A20R13 0683-0475 A20R14 0698-7268 A20R15 0757-0278	9 0 1 5 9	1 1 1 1	RESISTOR 100 1% 05W F TC=0+=100 RESISTOR 287 1% 125W F TC=0+=100 RESISTOR 4.7 5% 25W FC TC==400/+500 RESISTOR 21.5K 1% 05W F TC=0+=100 RESISTOR 1.78K 1% 125W F TC=0+=100	24546 24546 01121 24546 24546	C3=1/8=T0=100R=G C4=1/8=T0=287R=F C847G5 C3=1/8=T0=2152=G C4=1/8=T0=1781=F
A20R16 0698=7264 A20R17 0698=7253 A20R18 0698=7250 A20R19 0698=7257	1 8 7 2	1 3	RESISTOR 14.7K 1% .05W F TC=0+=100 RESISTOR 5.11K 1% .05W F TC=0+=100 RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 7.5K 1% .05W F TC=0+=100	24546 24546 24546 24546	C3=1/8=T0=1472=G C3=1/8=T0=5111=G C3=1/8=T0=1002=G C3=1/8=T0=7501=G
A207P1 0360=1514	7		TERMINAL-STUD SGL-PIN PRESS-MTG	26480	0360-1514
A20U1 1820=0247	8	1	IC V RGLTR TO=99	27014	LM305H
A20VR1 1902-3279 A20VR2 1902-0041	6 4	1	DIODE-ZNR 28.7V 5% DO-7 PD=.4W TC=+.078% DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=009%	28480 28480	1902-3279 1902-0041
1200=0173	=		A20 MISCELLANEOUS	38//84	1300-0133
1200=0173	8	1	INSULATOR=XSTR DAP=GL BRACKET=RTANG .438=LG x .781=LG .375=WD	28480 28480	1200=0173 1400=0263
A21 86603-60007	8	1	FILTER DRIVER ASSY	28480	86603-60007
A21C1 0160=4247 A21C2 0160=4247 A21C3 0160=4247 A21C4 0160=4247 A21C5 0160=4247	55555		CAPACITOR=FXD .047UF +=20% 100VDC CER	28480 28480 28480 28480 28480	0160=4247 0160=4247 0160=4247 0160=4247 0160=4247

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A21C6 A21C7 A21C8 A21C9 A21C10	0160-4247 0160-4247 0160-4247 0160-4247 0160-2055	5 5 5 5 9		CAPACITOR=FXD .047UF +=20% 100VDC CER CAPACITOR=FXD .047UF +=20% 100VDC CER CAPACITOR=FXD .047UF +=20% 100VDC CER CAPACITOR=FXD .047UF +=20% 100VDC CER CAPACITOR=FXD .01UF +80=20% 100VDC CER	28480 28480 28480 28480 28480	0160=4247 0160=4247 0160=4247 0160=4247 0160=2055
421C11 421C12 421C13 421C14	0160-4247 0160-4247 0160-0127 0160-0127	5 5 2 2		CAPACITOR-FXD .047UF +=20% 100VDC CER CAPACITOR-FXD .047UF +=20% 100VDC CER CAPACITOR-FXD 1UF +=20% 25VDC CER CAPACITOR-FXD 1UF +=20% 25VDC CER	28480 28480 28480 28480	0160=4247 0160=4247 0160=0127 0160=0127
A21CR1 A21CR2	1901-0033 1901-0033	5		DIODE-GEN PRP 180V 200MA DO-7 DIODE-GEN PRP 180V 200MA DO-7	28480 28480	1901-0033 1901-0033
A21L1	9140-0210	1	1	COIL-MLD 100UH 5% Q=50 .155Dx.375LG-NOM	28480	9140=0210
421Q1 A21Q2	1854-0023 1853-0038	9 4	1	TRANSISTOR NPN SI TO-18 PD=360MW TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ	28480 28480	1854=0023 1853=0038
A21R1 A21R2 A21R3 A21R4 A21R5	2100-2692 2100-2515 2100-2515 2100-2516 2100-2517	6 2 3 4	1 4 3	RESISTOR-TRMR 1M 20% C SIDE-ADJ 1-TRN RESISTOR-TRMR 200K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 200K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 100K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 50K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 50K 10% C SIDE-ADJ 1-TRN	30983 30983 30983 73138 30983	ET50X105 ET50W204 ET50W204 82PAR100K ET50X503
A21R6 A21R7 A21R8 A21R9 A21R10	2100-2514 2100-2515 2100-2515 2100-2516 2100-2516	1 2 3 3	S	RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 200K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 200K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 100K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 100K 10% C SIDE-ADJ 1-TRN	30983 30983 30983 73138 73138	ET50%203 ET50%204 ET50%204 82PAR100K 82PAR100K
A21R11 A21R12 A21R13 A21R14 A21R15	2100-2517 2100-2514 2100-2522 0757-0280 0698-7277	1 1 3 6	1 4	RESISTOR-TRMR 50K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 20K 10% C SIDE-ADJ 1-TRN RESISTOR-TRMR 10K 10% C SIDE-ADJ 1-TRN RESISTOR 1K 1% 125W F TC=0+000 RESISTOR 51.1K 1% .05W F TC=0+-100	30983 30983 30983 24546 24546	ET50×503 ET50×203 ET50×103 C4=1/8=T0=1001=F C3=1/8=T0=5112=G
A21R16 A21R17 A21R18 A21R19 A21R20	1810=0039 0698=7284 0698=7277 0698=7277 0698=7253	55668	1	NETWORK-RES 16-PIN-DIP .1-PIN-SPCG RESISTOR 100K 1% .05W F TC=0+-100 RESISTOR 51.1K 1% .05W F TC=0+-100 RESISTOR 51.1K 1% .05W F TC=0+-100 RESISTOR 5.11K 1% .05W F TC=0+-100	28480 24546 24546 24546 24546	1810=0039 C3=1/8=T0=1003=G C3=1/8=T0=5112=G C3=1/8=T0=5112=G C3=1/8=T0=5111=G
A21R21 A21R22 A21R23 A21R24 A21R25	0698-7260 0698-7260 0698-7277 0698-7243 0698-7229	7 7 6 6 8		RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 51.1K 1% .05W F TC=0+=100 RESISTOR 1.96K 1% .05W F TC=0+=100 RESISTOR 511 1% .05W F TC=0+=100	24546 24546 24546 24546 24546	C3-1/8-T0-1002-G C3-1/8-T0-1002-G C3-1/8-T0-5112-G C3-1/8-T0-1961-G C3-1/8-T0-511R-G
A21R26* A21R27 A21R28 A21R29 A21R30	0698-7288 0698-7240 0698-7258 0698-7253 0698-7229	3 8 8	1 1 1	RESISTOR 147K 1% .05W F TC=0+-100 RESISTOR 1.47K 1% .05W F TC=0+-100 RESISTOR 8.25K 1% .05W F TC=0+-100 RESISTOR 5.11K 1% .05W F TC=0+-100 RESISTOR 5.11 1% .05W F TC=0+-100	24546 24546 24546 24546 24546	C3=1/8=T0=1473=G C3=1/8=T0=1471=G C3=1/8=T0=8251=G C3=1/8=T0=5111=G C3=1/8=T0=511R=G
A21R31 A21R32 A21R33 A21R34 A21R35 A21R35 A21R36* †	0598-7248 0698-7260 0598-7267 0698-7267 0698-7270 0698-7236 0360-0124	1 7 7 4 9 7 3	1	RESISTOR 3.16K 1% .05W F TC=0+=100 RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 10K 1% .05W F TC=0+=100 RESISTOR 19.6K 1% .05W F TC=0+=100 RESISTOR 26.1K 1% .05W F TC=0+=100 RESISTOR 1K 18 .05W F TC=+-100 CONNECTOR=SGL CONT PIN .04=IN=BSC=SZ RND	24546 24546 24546 24546 24546 28480	C3-1/8-T0-31b1-G C3-1/8-T0-1002-G C3-1/8-T0-1002-G C3-1/8-T0-10902-G C3-1/8-T0-2612-G C3-1/8-T0-1003-G 0360-0124
A21U1 A21U2 A21U3 A21U4 A21U5	1820-0214 1820-1746 1820-1197 1820-1746 1820-0102	0 4 0 4 4	1 2 1	IC DOOR TTL BOD-TO-DEC 4-TO-10-LINE IC BFR CMOS INV HEX IC GATE TTL LS NAND QUAD 2-INP IC BFR CMOS INV HEX IC FF ECL J-K	01295 04713 01295 04713 04713	\$N7442AN MC14049BCP \$N74L500M MC14049BCP MC1013P
A21U6 A21U7 A21U8	1826=0161 1820=0175 1826=0013	7 1 8	1 1	IC 324 OP AMP 14-DIP=P IC INV TTL HEX 1-INP IC 741 OP AMP TO-99	18324 01295 06665	LM324-A SN7405N SSS741CJ
A21VR1	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC==.009%	28480	1902-0041
				A21 MISCELLANEOUS		
	0340-0044 4040-0748	3		TERMINAL-STUD DBL-TUR PRESS-MTG EXTRACTOR-PC BOARD BLK POLYC	28480 28480	0340=0044 4040=0748
\$ 5 \$ \$ \$ \$	86603=60053 86603=60054	4 5	1 1	FREQUENCY DOUBLER ASSY RESTORED 86603=60053,REQUIRES EXCHANGE A22 MISCELLANEOUS	28480 28480	86603-60053 86603-60054
	86603-00006		1 1	COVER, DOUBLER/AMPLIFIER COVER, DOUBLER	28480 28480	86603=00006 86603=00012

Table 6-3. Replaceable Parts

Reference Designation			Description	Mfr Code	Mfr Part Number	
42241	86603-60006	7	1	DOUBLER/FILTER ASSY	28480	86603-60006
# S4554	86603-60027	5	1	DOUBLER AMPLIFIER ASSY NO. 1	28480	86603-60027
A2243 T	86603-60047	6	1	DOUBLER AMPLIFIER ASSY NO. 2	28480	86603=60047
A22A4	86603-60008	9	1	OUTPUT DETECTOR ASSY	28480	86603-60008
42245	80003-60030	7	1	RELAY ASSY	28480	86603=60030
423	85603-60034	1	1	DOUBLER SWITCH ASSY (OPTION 003 ONLY)	28480	86603-60034
A2301	1854-0071	7		TRANSISTOR NPN SI PD=300Mw Ft=200MHZ	28480	1854-0071
A23R1	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0+=100	24546	C4-1/8-T0-6811-F
A 2 3 S 1	3101-1299	0	1	SWITCH-PB DPDT ALTNG .454 115VAC	28480	3101-1299
42301	1820-0054	5		IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
A 2 4	86603-60045	4	1	FREQUENCY DOUBLER TEST SWITCH ASSY (OPTION 003 ONLY)	28480	86603-60045
A24CR1 A24CR2	1910=0016 1910=0016	0	4	DIODE-GE 60V 60MA 1US DO-7 DIODE-GE 60V 60MA 1US DO-7	28480 28480	1910-0016
A24CR3	1910-0016	0		DIODE-GE 60V 60MA 1US DO-7	28480	1910=0016
A2451	3101-0903	1	2	SWITCH-SL DP3T-NS MINTR .54 125VAC/DC	28480	3101=0903
				CHASSIS PARTS		
174	0960-0084 0955-0058	6	1 1	ISOLATOR COAXIAL ATTENUATOR, 3D8 (OPTION OOZ ONLY)	28480 28480	0960=0084 0955=0058
C 1 C 2	0160=2437 0160=2437	1		CAPACITOR-FDTHRU 5000PF +80 -20% 200V CAPACITOR-FDTHRU 5000PF +80 -20% 200V	28480 28480	0160=2437 0160=2437
C 3	0160-2437	1		(EXCEPT OPTION 001) CAPACITOR-FOTHRU 5000PF +80 -20% 200V (EXCEPT OPTION 001)	28480	0160-2437
Cu	0160-2437	1		CAPACITOR-FDTHRU 5000PF +80 -20% 200V	28480	0160=2437
C 5	0160-2437	1		(EXCEPT OPTION 001) CAPACITOR-FOTHRU 5000PF +80 -20% 200V	28480	0160=2437
C 6	0160-2437	1		(EXCEPT OPTION 001) CAPACITOR - FOTHRU 5000PF +80 -20% 200V	28480	0160=2437
cat.	0160-2436	0	5	CAPACITOR-FOTHRU 10PF 20% 200V CER	28480	0160-2436
C9 T	0180-0116 0180-0116 0160-2436	1 1 0		CAPACITOR=FXD 6.8UF+=10% 35VDC TA CAPACITOR=FXD 6.8UF+=10% 35VDC TA CAPACITOR=FOTHRU 10PF 20% 200V CER (OPTION 003 ONLY)	56289 56289 28480	1500685x903582 1500685x903582 0160-2436
C ₁₁	0160-2436	0		CAPACITOR-FOTHRU 10PF 20% 200V CER	28480	0160-2436
C12	0160-2436	0		(OPTION 003 DNLY) CAPACITOR=FDTHRU 10PF 20% 200V CER	28480	0160-2436
C 1 3	0160-2436	0		(OPTION 003 ONLY) CAPACITOR-FDTHRU 10PF 20% 200V CER (OPTION 003 ONLY)	28480	0160=2436
CP1	1910-0016	0		DIODE-GE 60V 60MA 1US DO-7 (EXCEPT OPTION 001)	28480	1910=0016
DS1	2140-0092	0	1	LAMP-INCAND 685 5VDC 60MA T-1-BULB	0000J	685 TIP END
	1450-0371 1450-0153	4 0	1 1	LENS CAP AMS=TL .219=DIA 12=40 THD LAMPHOLDER MOGT=SC=FLG=SKT TUH=TERM	28480	1450=0371 1450=0153
FL1	9135-0009	5	1	FILTER-ELEC 8P: 4GHZ CTR FREQ	28480	9135=0009
J1 J1				OUTPUT JACK, TYPE N(EXCEPT OPTION 001; P/O A13;SEE MP1) OUTPUT JACK,TYPE N(OPTION 001 ONLY;INCL MP2 THRU MP9)		
L1+ L2+ L3+ L4+	9100=1640 9100=1629 9170=0499 9170=0499	9 4 1 1	1 1 2	COIL-MLD 160UH 5% G=65 .155Dx.375LG-NOM COIL-MLD 47UH 5% G=55 .155Dx.375LG-NOM CORE-TOROID AL=2135-NH/7 CORE-TOROID AL=2135-NH/7	28480 28480 28480 28480	9100=1640 9100=1629 9170=0499 9170=0499
м1	1120-0543	3	1	METER METER; 1MA; 2.5-IN CASE; 147 OHM	28480	1120=0543
MP1	08731=210 2950=0132	5	1 1	NUT, LOCK(EXCEPT OPT 001, P/O J1) NUT=HEX=DBL=CHAM 7/16=28=THD .094=IN=THK	28480	08731=210 ORDER BY DESCRIPTION
мр з	1250-0914	7	1	(OPT 001 ONLY, P/O J1) CONNECTOR-RF APC-N FEM UNMID 50-OHM (OPT 001 ONLY, P/O J1)	28480	1250=0914

Table 6-3. Replaceable Parts

Reference HP Part Number					Mfr Code	Mfr Part Number	
мр ц	1250-0915	8	1	CONTACT-RF CONN SER APC-N FEMALE	02650	131-149	
MP5	5040-0306	0	1	(OPT 001 ONLY, P/O J1) INSULATOR	28480	5040=0306	
~ Pb	08555-20093	5	1	(OPT 001 ONLY, P/O J1) CONTACT, JACK (OPT 001 ONLY, P/O J1)	28480	08555-20093	
wp 7	08761-2027	4	1	INSULATOR (OPT 001 ONLY, P/O J1)	28480	08761-2027	
W P B	08555-20094	6	1	BODY, BULKHEAD	28480	08555=20094	
4P9	2190+0104	0	1	(OPT 001 ONLY, P/O J1) WASHER-LK INTL T 7/16 IN .439-IN-ID (OPT 001 ONLY, P/O J1)	28480	2190=0104	
MP10	1251-0546	3	1	CONN: REP CONT: RECT SER: COAXSKT	81312	III-170548	
P11	1250+1193	6	3	(P/O wi7, w20, ww21; 2 EACH) CONNECTOR-RF SW-SLO FEM UNMTD 50-OHM	28480	1250-1193	
4P12	1250-1221	1	1	(P/O w9, w12, w18, w19; 1 EACH) CONNECTOR=RF SM=SLD M SGL=HOLE=REC (P/O w3 & w11, 1EA,;INCLUDES P1, P2)	28480	1250=1221	
MP13	1250+0872	6	1	CONNECTOR-RF SMB FEM UNMTD 50-0HM	28480	1250=0872	
MP14	1250+1227	7	1	(P/O W15, 1 EA.;P/O W14 & W16; 2 EA) CONNECTOR=RF SMA M UNMTD 50=OHM	28480	1250=1227	
MP15	0362=0387	4	1	(P/O W3,W11, & W15; 1 EACH) SLEEVE=METAL .179=OD CU .138=ID .375=LG (P/O W3, W11, W14, W15, & W16; 2 EA)	28480	0362=0387	
21				NSR, P/O MP12			
) }	1251-2293	1	4	NSR, P/O MP12 CONNECTOR=SGL CONT SKT _032=IN=BSC=SZ	28480	1251=2293	
95	1251-2293	1		CONNECTOR-SGL CONT SKT .032=IN+BSC+SZ CONNECTOR-SGL CONT SKT .032=IN+BSC+SZ	28480 28480	1251=2293	
26	86607-60044	4		(PART OF A14)	78.000	84407-40011	
0	5040-0382	2	1	CONNECTOR ASSY(INCL W8, W9, W17-W21) CONNECTOR BODY	28480 28480	86603-60011 5040-0382	
	5040+0383 1251-1911 1251+3087	8	8	CONNECTOR FACE CONTACT=CONN FEM CRP .062=IN=CONT=SZ CONTACT=CONN U/w=RECT FEM CRP	28480 28480 28480	5040=0383 1251=1911 1251=3087	
7	1251-2293	1		CONNECTOR=SGL CONT SKT .032=IN=B9C=SZ (PART OF A14)	28480	1251-2293	
212				NOT ASSIGNED			
013	1251=2262	4	1	CONNECTOR-PC EDGE 10-CUNT/ROW 2-ROWS (PART OF A14)	28480	1251=2262	
214	1251=2500	3	1	CONNECTOR PC EDGE 6=CONT/ROW 2=ROWS (PART OF A14)	28480	1251=2500	
3 1	1854-0072 86603-20048	8	1 1	TRANSISTOR NPN 2N3054 SI TO-66 PD=25w Insulator, Transistor TO-66	01928 28480	2N3054 86603=20048	
₹1 ₹2	2100-3113	8 5	1 1	RESISTOR=VAR CONTROL CCP 2.5K 10% 10CW RESISTOR 21.5 1% .125W F TC=0+=100	01121	WA4G0363252AZ PME55-1/8-10-21R5-F	
51	3100=3050	3	1	SWITCH-ROTARY SW-RTRY	28480	3100=3050	
31	3100=3088	7	1	(EXCEPT OPTION 001) SWITCH, ROTARY (OPTION 001 ONLY)	28480	3100-3088	
32	3101-0903	1		SWITCH-SL DP3T-NS MINTR .5A 125VAC/DC (EXCEPT OPTION 003)	28480	3101-0903	
re1	0360=1780	9	1	TERMINAL STRIP 5-TERM PHEN 1,25-IN-L	28480	0360=1780	
v 1 v 1	86603-20012	1	1	CABLE ASSY, FILTER OUTPUT(OPT 002 ONLY) CABLE ASSY, FILTER OUTPUT	28480 28480	86603=20012 86603=20038	
15	86603-20037 86603-20014	0	1 1	(EXCEPT OPTION 002) CABLE ASSY, MIXER INPUT(EXCEPT OPT 002) CABLE, MIXER LO INPUT(OPT 002 ONLY)	28480	86603-20037 86603-20014	
v 3	86603-60013		1	CABLE ASSY, RF INPUT	28480	86603=60013	
v q	86603-20016		1	(INCLUDES MP12, MP14 AND MP15) CABLE ASSY, ISOLATOR OUTPUT	28480	86603-20016	
N 6	86603-20017		1 1	CABLE ASSY MIXER RF INPUT CABLE ASSY, MIXER OUTPUT	28480	86603-20015 86603-20017	
4 7 4 7	86603-20021	2	1	CABLE ASSY, OUTPUT (EXCEPT OPT 001) CABLE ASSY, OUTPUT (OPTION 001 ONLY)	28480 28480	86603-20021	
N.A.	86602-60012	4	i	CABLE ASSY, AM INPUT, GRAY/YELLOW (INCLUDES MP10, P/O P6)	28480	86602-60012	
• 9	86602-60021	5	1	CABLE ASSY, PULSE INPUT, WHITE/GREEN (INCLUDES MP10 & MP11, P/O P6)	28480	86602-60021	
910 911	86603-20013	2 7	1	CABLE, 4GMZ AMPLIFIER INPUT(OPT 002 ONLY) CABLE ASSY, LO INPUT	28480	86603-20013	
v12	86603-60015	8	1	(INCLUDES MP12, MP14 AND MP15) CABLE PHASE MOD DRIVER INPUT(OPT 002 ONL	25480	86603=60015	
				INCLUDES MP10 AND MP13)			

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
15	86603-20036	9	1	CABLE ASSY, CIRCULATOR INPUT	28480	80603-20030
14	8003-00012	5	1	(OPTION 002 ONLY) CABLE, PHASE DRIVER OUTPUT(OPT 002 ONLY,	28480	80003-00012
15	6003-00017	0	1	INCLUDES MPIS AND MPIS) CABLE, 1.3 AMPL OUTPUT INCLUDES MPIS, MPI4 AND MPIS)	28480	86603-60017
16	6003-00010		1	CABLE ASSY, DOUBLER INPUT(INCL MP138MP15 CABLE ASSY, 100 MMZ, AMITE/BROWN	28480	800300010
1 ē	60002-00034		1	(P/O Pb; SEE MP10) CABLE ASSY, 20 MMZ OUTPUT, MMITE/RED (P/O Pb; INCLUDES MP10 AND MP11)	28480	86602-60034
19	86602-69033	g	1	CABLE ASSY, 20 MHZ INPUT, MMITE/BLUE	28480	8000200033
	66602+60047		1	(P/O Pb, INCLUDES MP10 AND MP11) CABLE ASSY, 20/30 MMZ, MMITE/ORANGE	28480	86602-60047
21	50002-00048		1	(P/O Pe; SEE HP(0) CABLE ASSY,360/450 MMZ, MHITE/YELLON	28480	80002-000-8
151	1251-0194	7	1	(P/O P6) SEE MP10) CONNECTOR-PC EDGE 15-CONT/ROW 1-ROW	28480	1251-019-
*61	123130173	ľ	·	(P/O A14)		
				MISCELLANEOUS PARTS		
	0340-0189	8	1	INSULATOR-COVER NEOPRENE	28480	0340+0189 0370+1089
	0370-1089	0	1	KNOS-BASE 1/2 JGK ,125-IN-IO KNOS-BASE-PTR-AND-BAR 1/2 JK .25-IN-ID (OPTION 001 ONLY)	28480	0370-2994
	0370=279=	ê	1	KNOB, OUTPUT RANGE SHITCH (EXCEPT OPT 001)	28480	0370-2796
	0380-0045	[5	SPACER-RND .875-IN-LG .114-IN-ID	28480	0380+0045
	1251-1911 2190-0067	9	1	CONTACT-COMM FEW CRP ,062-IN-CONT-82 HASHER-LK INTL T 1/4 IN ,256-IN-IO (OPTION 003 ONLY)	28480	1251=1911 2190=0067
	2950-0052	q	1	NUT-HER-08-00-14-40-700 000-14-74K	30000	ORDER BY DESCRIPTION
	3050-0029 3050-0090	3	1	maswerafi wilc 3/8 IN .378=Ih=ID masweraspr mayy 5/8 IN .64=IN=ID (Except OPTION 001)	28480 28480	3050=0029 3050=0090
	86501+00013 86601+00014		1 1	GRACKET, ATTENUATOR	28480	86601-00013 86601-00014
	86601-00034	3	1	(EXCEPT OPTION 001) PANEL, FRONT (EXCEPT OPTION 001)	28480	80001-00034
	80001-00036	5	1	WOUNT, METER	28480	85501-00035
	86601-00052	5	2	COVER, MALF HOUSING, FRONT	28480	86601=00052
	86601-20019	1	1	(EXCEPT OPTION 003) STUD LATCH	28480	85501=20019
	86601-20020	0		HASHER LATCH	28480	05001-20020
	86601-20069	b	1	FRAME, FRONT PANEL	28480	85601-20069
	86601=20080	7	1	GUIDE, PLUG-IN SCREM, METER ADJUST	28480	86601=40018
	80002-00005			SUPPORT, TOP	28480	86602*00005
	8002-00006			SUPPORT, BOTTON PANEL, PRONT (OPTION 001 ONLY)	28480	85502=00005 85502=00007
	86602-00007	7	2	PLATE, FRONT SUPPORT	28480	91005=20068
	85503-20028			GUIDE, CONNECTOR SUPPORT, RIGHT FRONT	28480 28480	85502=20028
	86603-00002	7			28480	80003-00002
	86603-00003	8	1	SUPPORT, MIXER	28480	8003=00003
	8003-00008 8003-00009 8003-00011	4	1	SUPPORT, LEFT CLAMP (OPTION 002 ONLY) PANEL, FRONT (OPTION 003 ONLY)	28480 28480 28480	86603-00009
	86603-20018		1	SUPPORT, DOUBLER HOUSING	28480	86903=20018 86903=20020
	86603-20020			MINDOM (EXCEPT OPTION GOZ) PANEL, REAR	28480	86603-20025
	86603-20026	7	1	HOUSING, FRONT (OPTION 003 ONLY) PLATE, REAR SUPPORT	28480	86603-20026 86603-20028
	80003-20028		1	HINDON (OPTION OOZ ONLY)	28480	
	00003*20035			1000 (0.100) 001 001		

Table 6-4. Code List of Manufacturers

Mfr			T
Code	Manufacturer Name	Address	Zip Code
000CJ 000CJ 000CJ 0129C 0129R 02112 0266C 03888 04713 06665 16546 24546 26654 24546 26654 27014 28480 35763 56289 73138 73138 73138 96341	GTE SYLVANIA MINIATURE LT PROD ANY SATISFACTORY SUPPLIER ALLEW-SRADLEY CO TEAS INST INC SEMICOND CMPNT DIV PCA COAP SOLID STATE DIV SPECIFOL ELECTRONICS COAP PSICHTLE COAP NOTIFICA SEMICONDUCTOR PRODUCTS PRECISION MONOLITHICS INC US CAPACITOR COAP SIGNETICS COAP COMING GLASS MOPKS (BRADFORD) VARATYE INC VARATYE INC VARATYE INC SPECIFOL COAP RECLETTA COAP RECLETA COAP REC	HILLSBORO NH .S. MILWAUKEE WI DALLAS TX SOMERVILLE NJ CLTY OF IND CA BROADVIEW IL WHIPPANY NJ PHOENIX AZ SANTA CLARA CA BURBANK CA SANTA CLARA CA CAZENOVIA NY NORTH ADAWS MA HILLIMANTIC CT FULLERTON CA ATTLEBORO MA DAVILLE CT BURLINGTON MA	03244 53204 75222 08876 91745 60153 07981 85062 95050 91504 94086 16701 90404 95051 94304 92121 13035 01247 06226 92634 02703 06779 01803

Model 86603A Manual Changes

SECTION VII MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains manual change instructions for backdating this manual for HP Model 86603A RF Sections that have serial number prefixes that are lower than the last prefix listed on the title page.

7-3. MANUAL CHANGES

7-4. To adapt this manual to your instrument, refer to Table 7-1 and make all of the manual changes listed opposite the instruments serial number or prefix. The manual changes listed in

serial number sequence and should be made in the sequence listed. For example, Change A should be made after Change B; Change B should be made after Change C, etc. Table 7-2 is a summary of changes by component.

7-5. If the serial number of the instrument is not listed on the title page of this manual, or in Table 7-1, it may be documented in a yellow MANUAL CHANGES supplement. For additional important information about serial number coverage, refer to INSTRUMENTS COVERED BY MANUAL in Section I.

Table 7-1. Manual Changes by Serial Number

Serial Prefix or Number	Make Manual Changes
1417A	R thru A
1501A	R thru B
1505A	R thru C
1515A	R thru D
1521A0091 thru 1521A00220	R thru E
1521A00221 thru 1521A00240	R thru F
1533A	R thru G
1539A	R thru H
1543A	R thru I
1550A00311 thru 1550A00431, 1550A00433 thru 1550A00437, 1550A00439 thru 1550A00462, 1550A00470 thru 1550A00474, 1550A00476,	R thru J

Serial Prefix or Number	Make Manual Changes
1550A00478 and 1550A00479	R thru J (cont'd)
1550A00463 thru 1550A00469, and 1550A00477	R thru K
1625A	R thru L, J
1637A	R thru K
1638A	R thru M, K
1639A	R thru L
1640A	R thru M
1653A	R thru N
1734A	R thru O
1816A	R thru P
1847A	R,Q
1921A	R

Table 7-2. Summary of Changes by Component

Change	A2	A9	A11	A16	A17	A17A1	A20	A21	A22	A22A2	A22A3	Chassis
A										Ass'y Part No.	Ass'y Part No.	
В												C8, C9 L1, L2
С											Ass'y Part No.	
D		R5, R6, R15, R16, R25. R26										
E								U8				
F												L2
G				Assembly Part No.								
Н					C1, C2 C3, CR1, CR2	Assembly Part No.						
I		R9, R10, R19, R29, R30, R40										
J											R3, R7	
K			U7									
L							R15		R3		R3, R7, R8, R11	
M										C1, C13	C1	
N		Assembly Part No.										
0												L3
P												L4
Q								R36				
R	R9											

NOTE

Be sure to check the serial number of your instrument against Table 7-1 to see which changes apply.

7-6. MANUAL CHANGE INSTRUCTIONS

CHANGE A

Table 6-3 and Service Sheet 7:

Change the part numbers of A22A2 and A22A3 to 86603-60005.

CHANGE B

Page 6-14, Table 6-3:

Change C8 to 0160-3451, CAP-FXD 0.01 UF +80 -20% 100 WVDC CER, 28480, 0160-3451.

Change C9 to 0180-2141, CAP-FXD 3.3 UF ±10% 50 VDC TA, 56289, 150D335X9050B2.

Change L1 and L2 to 9140-0210, COIL FXD MOLDED RF CHOKE 100 UH 5%, 24226, 15/103.

Service Sheet 6:

Show C8 (now 0.01 UF) connected from the junction of L1 and L2 to ground.

Change C9 to 3.3 UF.

CHANGE C

Table 6-3 and Service Sheet 7:

Change the part number of A22A3 to 86603-60047.

CHANGE D

Page 6-9, Table 6-3:

Change A9R5, R6, R15, R25, and R26 to 0811-2815, RESISTOR 1.5 OHM 5%, 0.5W TUBULAR, 91637, RS1/2-T2-IR5-J.

Service Sheet 9:

Change the value of A9R5, R6, R15, R16, R25 and R26 to 1.5 ohm.

CHANGE E

Table 6-3 and Service Sheet 10:

Change the part numbers of A21U8 to 1826-0013.

CHANGE F

Page 6-15, Table 6-3:

Change L2 to COIL-FXD MOLDED RF CHOKE 160 UH 5%.

Page 8-31, Figure 8-17 (Service Sheet 6):

Change the value of L2 to 160 UH.

CHANGE G

Page 5-9, Figure 5-6:

Replace figure with Figure 7-1.

Page 5-10, paragraph 5-29:

Change the procedure as follows:

3. Set the sweep generator controls as follows: sweep range to 110 MHz, frequency to 80 MHz, output level at -10 dBm, sweep video, and sweep mode free-slow.

CHANGE G (Cont'd)

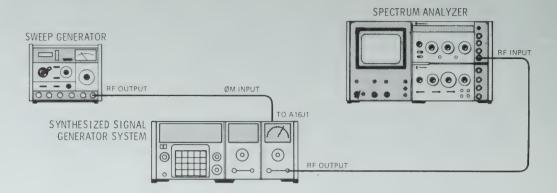


Figure 7-1. Phase Modulator Driver Frequency Response Adjustment Test Setup (Change G)

Page 5-10, procedures (cont'd):

- 6. Set the spectrum analyzer controls for center frequency of 1.05 GHz, frequency span per division 20 MHz, resolution bandwidth 300 kHz, input attenuation 30 dB, vertical sensitivity per division 10 dB, and sweep time per division 2 ms.
- 7. Adjust the sweep generator output level so the sidebands are approximately 34 dB below the carrier level.
- 8. Set the spectrum analyzer vertical sensitivity per division to 2 dB.
- 9. Adjust the Frequency Response control (A16C8) for maximum flatness within 40 MHz of the carrier and for the minimum peaking at 80 MHz.
- 10. Disconnect the sweep generator from the A16 Assembly and set the signal generator LINE switch to STBY.
- 11. Carefully remove the RF Section. Be careful not to damage the cables. Reconnect W12 to A16J1.

Page 5-11, Figure 5-8:

Change the reference "step 15" to step "13" in two places.

Page 5-11, paragraph 5-30:

Change the last sentence of step 2 to: "Be sure to use the correct test oscillator output and the correct low pass filter".

Page 5-12, paragraph 5-30:

Change the procedure as follows:

8. Set the spectrum analyzer controls for a center frequency of 100 MHz, resolution bandwidth of 10 kHz, frequency span per division of 0.5 MHz, sweep time per division 10 ms, input attenuation of 30 dB, vertical scale per division to 2 dB, and adjust the reference level to a readable level.

Model 86603A Manual Changes

MANUAL CHANGES

CHANGE G (Cont'd)

9. Adjust A16R4 one-eighth turn counterclockwise. If A16R4 is in contact with the ccw stop, increase the value of A16R5.

NOTE

The normal value range is 10 to 316 ohms.

Set the frequency of the System Under Test to 100 MHz and repeat steps 7 and 8.

10. Adjust A16R4 one-eighth turn clockwise. If A16R4 is in contact with the cw stop, decrease the value of A16R5.

NOTE

The normal value range is 10 to 316 ohms.

Set the frequency of the System Under Test to 100 MHz and repeat steps 7 and 8.

- 11. Set the FM discriminator controls for the 10 MHz range, and 0.1V sensitivity. Insert an internal 1 MHz low pass filter.
- 12. Set the spectrum analyzer controls for a center frequency of 200 kHz, resolution bandwidth to 3 kHz, frequency span per division to 50 kHz, input attenuation to 0 dB, log reference level to a convenient level, vertical sensitivity per division to 10 dB, and scan time per division to 10 ms.
- 13. Set the Reference System controls for a center frequency of 309 MHz and an output level of +7 dBm.
- 14. Set the System Under Test center frequency to 300 MHz with a modulation level of 100° as read on the front panel meter.

Page 5-13, paragraph 5-30:

Change the procedure as follows:

- 15. Refer to Figure 5-8 and connect the System Under Test OUTPUT to the RF input of the mixer. Connect the FM Discriminator output to the spectrum analyzer RF input.
- 16. Adjust the spectrum analyzer reference level control until the peak of the fundamental 100 kHz signal is viewed on the CRT display at the log reference graticule line.
- 17. Adjust A16R3 to null the second harmonic level; adjust A16R1 to null the third harmonic level.

NOTE

After passing through an FM discriminator, the harmonic distortion of a ϕM signal will increase in level of 6 dB per octave. Therefore, the second harmonic will be 6 dB higher and the third harmonic 9.5 dB higher than with a phase demodulator.

18. Step the System Under Test center frequency down 1 Hz. Note the direction and amount of readjustment of A16R3 and R1 necessary to null the second and third harmonics.

CHANGE G (Cont'd)

- 19. Set A16R3 and R1 for the best compromise (minimum second and third harmonic levels) at both center frequency settings of 299.999999 and 300 MHz.
- 20. Repeat steps 4 through 20 until all the following conditions are met without further adjustment.
 - a. Carrier and first sidebands equal within 0.5 dB when changing Center Frequency of System Under Test between 100 and 99.999999 MHz (steps 7 and 8).
 - b. Second harmonic levels are equal within 4 dB or >40 dB down from the fundamental as indicated by the spectrum analyzer at center frequencies of 300 and 299.99999 MHz (Step 19).
 - c. Third harmonic levels are equal within 4 dB or >35 dB down from the fundamental as indicated by the spectrum analyzer at center frequencies of 300 and 299.999999 MHz (Step 19).
- 21. Replace the mainframe cover and wait 10 minutes. Check that the conditions outlined in step 20 are still met. If not, repeat steps 4 through 20.

Delete steps 22 and 23.

Page 5-14, Figure 5-9:

Change the reference "step 11" to "step 13".

Change the second sentence of step 2 to "Be sure to use the correct test oscillator output and the correct low pass filter."

Page 5-15, paragraph 5-31:

Change the procedure as follows:

- 8. Adjust A16R2 until the carrier and first sidebands are of equal amplitude.
- 9. Step the System Under Test center frequency down 1 Hz to 99.999999 MHz. The carrier and first sidebands should be within 0.5 dB. If the difference is less than or equal to 0.5 dB, proceed to step 11. If the difference is greater than 0.5 dB, and if the ϕ M deviation is $<82^{\circ}$ (first sideband is of lower amplitude than the carrier) proceed to step 9. If the ϕ M deviation is $>82^{\circ}$ proceed to step 10.
- 10. Adjust A16R4 one-eight turn clockwise. If A16R4 is in contact with the cw stop, decrease the value of A16R5.

NOTE

The normal value range is 10 to 316 ohms.

Set the frequency of the System Under Test to 100 MHz and repeat steps 7 and 8.

- 11. Set the spectrum analyzer controls for a center frequency of 2 MHz, resolution bandwidth to 30 kHz, frequency span per division to 0.5 MHz, input attenuation to 0 dB, log reference level to a convenient level, vertical sensitivity per division to 10 dB, and scan time per division to 10 ms.
- 12. Set the System Under Test center frequency to 300 MHz with a modulation level of 100° as read on the front panel meter.

Model 86603A Manual Changes

MANUAL CHANGES

CHANGE G (Cont'd)

- 13. Connect the phase modulation test set between the signal generator output and the spectrum analyzer input as shown in Figure 5-9.
- 14. Adjust the spectrum analyzer reference level until the peak of the fundamental 1 MHz signal is viewed on the CRT display at the log reference graticule line.
- 15. Adjust A16R3 to null the second harmonic level; adjust A16R1 to null the third harmonic level.
- 16. Step the System Under Test center frequency down 1 Hz. Note the direction and amount of readjustment of A16R3 and R1 necessary to null the second and third harmonics.
- 17. Set A16R3 and R1 for the best compromise (minimum second and third harmonic levels) at both center frequency settings of 299.999999 MHz and 300 MHz.
- 18. Repeat steps 4 through 17 until all the following conditions are met without further adjustment.
 - a. Carrier and first sidebands are equal within 0.5 dB when changing center frequency of System Under Test, between 100 and 99.999999 MHz (steps 7 and 8).
 - b. Second harmonic levels are equal within 4 dB or >40 dB down from the fundamental at center frequencies of 300 and 299.99999 MHz (step 17).
 - c. Third harmonic levels are equal within 4 dB or > 35 dB down from the fundamental at center frequencies of 300 and 299.999999 MHz (step 17).
- 19. Replace the mainframe cover and wait 10 minutes. Check to see if the conditions outlined in step 18 are still met. If not, repeat steps 4 through 18.

Delete steps 20 and 21.

Page 6-2, Table 6-1:

Add A22A2 (reference designation), Doubler Amplifier Assembly No. 1 (Description), 86603-60031 (Exchange Assembly), and 86603-60027 (New Assembly).

Page 6-11, Table 6-3:

Change the parts list for the A16 Assembly as shown in this section.

Page 8-29, Figure 8-15 (Service Sheet 5):

Replace Figure 8-15 with Figure 7-2.

CHANGE H

Page 6-12, Table 6-3:

Change:

A17C1 to A17A1C1

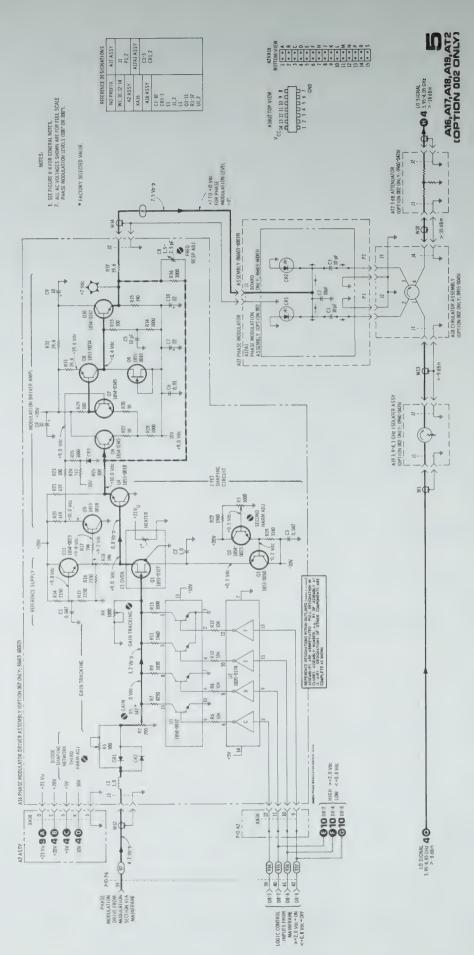
A17C2 to A17A1C2

A17C3 to A17A1C3

A17CR1 to A17A1CR1

A17CR2 to A17A1CR2

Add A17A1, 86603-60003, 1, PHASE MODULATOR BOARD ASSY, 28480, 86603-60003.



CHANGE H (Cont'd)

Page 8-29, Figure 8-17 (Service Sheet 5):

Change the diagram as shown in the partial schematic.

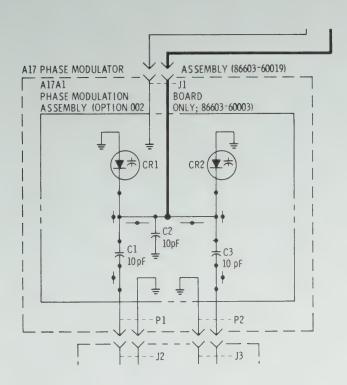


Figure 7-3. Phase Modulator Assembly (P/O Change H)

CHANGE I

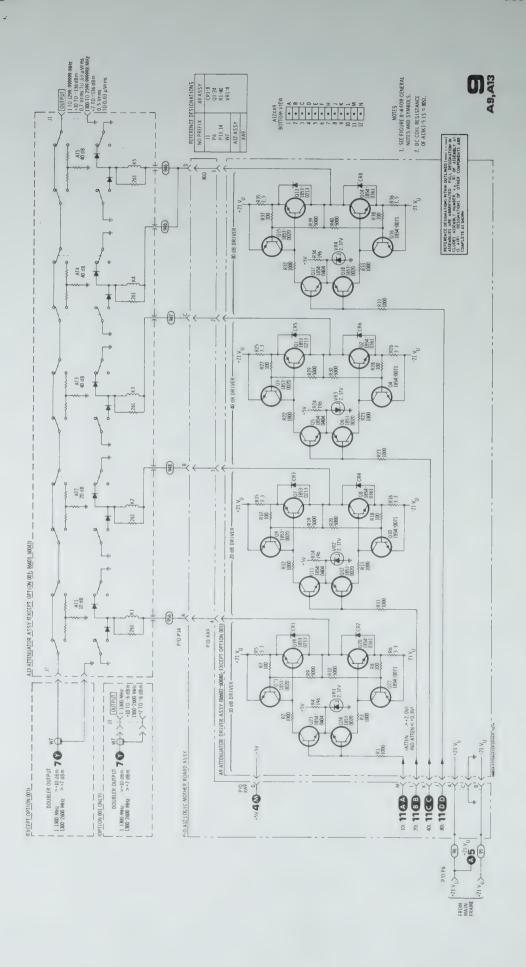
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Page 6-9, Table 6-3:
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Add A9R9, 0698-4002, RES: 5K 1% 0.125W F TC=0 ±100, 16299, C4-1/8-TO-5001-F A9R10, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R19, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R20, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R29, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R30, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R39, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R40, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R40, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F A9R40, 0698-4002, RES: 5K 1% 0.125W F TC = 0±100, 16299, C4-1/8-TO-5001-F
```

Page 8-37, Figure 8-25 (Service Sheet 9): Replace Figure 8-25 with Figure 7-4.

CHANGE J

Page 8-33, Figure 8-19 (Service Sheet 7): Change A22A3R3 and A22A3R7 to 162 ohms.



CHANGE K

Page 6-10, Table 6-3:

Change A11U7 to 1820-0639.

Page 8-41, Figure 8-30 (Service Sheet 11):

Change the diagram as shown in the partial schematic.

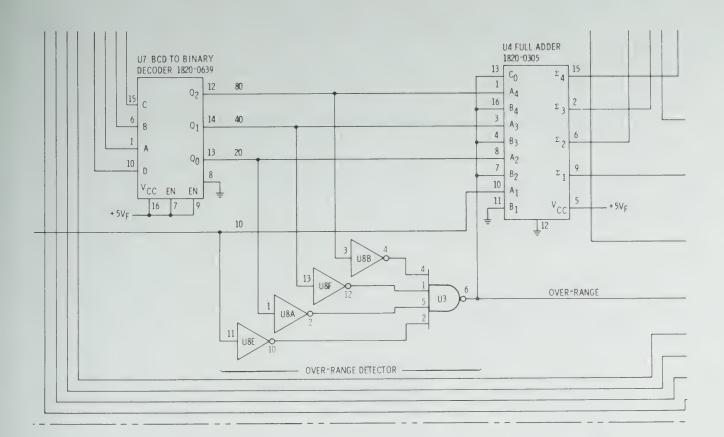


Figure 7-5. Service Sheet 11 Partial Schematic (P/O Change K)

CHANGE L

Page 6-13, Table 6-3:

Change A20R15 to 0698-7241, 1, RESISTOR 1.62K 2% 0.05W F TC=0±100, 16299, C3-1/8-TO-1621-G.

Page 8-33, Figure 8-19 (Service Sheet 7):

Change A22A3R3 and A22A3R7 to 162 ohms.

Change A22A3R8 and A22A3R11 to 909 ohms.

Add a 26.1 ohm resistor (A22R3) in the line between A22A2C12 and A22A3C12.

Page 8-43, Figure 8-32 (Service Sheet 12):

Change A20R15 to 1620 ohms.

CHANGE M

Page 8-33, Figure 8-19 (Service Sheet 7):

Change A22A2C1 and A22A3C1 to 2.2 pF.

Delete A22A2C13.

CHANGE N

Page 6-8 and 6-9, Table 6-3:

Replace the parts list for A9 Attenuator Driver Assy with Table 7-3 Replaceable Parts (Part of Change N).

Page 8-37, Figure 8-24:

Replace the figure with Figure 7-6, Component Locations Diagram (Part of Change N).

Page 8-37, Figure 8-25 (Service Sheet 9):

Replace the schematic with Figure 7-7, Schematic Diagram (Part of Change N).

CHANGE O

Page 6-15, Table 6-3:

Delete L3 under CHASSIS PARTS.

Page 8-27, Figure 8-12 (Service Sheet 4):

Delete L3 between A12P13 pins 9, K and P5.

CHANGE P

Page 6-15, Table 6-3:

Delete L4 under CHASSIS PARTS.

Page 8-43, Figure 8-32 (Service Sheet 12):

Delete L4 between green (5) wire and base of Q1.

Table 7-3. Replaceable Parts (Part of Change N) (1 of 2)

9	86602=60040	8	i	ATTENUATOR DRIVER ASSY (EXCEPT OPTION 001)	28480	86602-60040
49CH1	1901-0025	2	8	DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
49022	1901-0025	5	- 1	DIODE-GEN PRP 100V 200MA 00-7	28480	1901-0025
49603	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
AGCRU	1901-0025	2		DIDDE-GEN PRP 100V 200MA DO-7	28480	1901-0025
49085	1901-0025	5		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
49096	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901=0025
A 3 (2 7	1901-0025	5		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
4 9 C 2 A	1901-0025	2		DIODE-GEN PRP 100V 200MA DO-7	28480	1901-0025
4941	1853-0213	7	4	TRANSISTOR PNP 2N4236 SI TO-5 PD=1W	04713	2N4236
4942	1854-0361	8	4	TRANSISTOR NPN 2N4239 SI TO-5 PD=800MW	04713	2N4239
4963	1853-0020	4	8	TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
46147	1854-0071	7	4	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
4965	1854-0404	0	ш	TRANSISTOR NPN 31 TO-18 PD=360MW	28480	1854-0404
4965	1853-0020	4		THANSISTOR PNP SI PD=300Mw FT=150MHZ	28480	1853-0020
4947	1853-0213	7		TRANSISTOR PNP 2N4236 SI TO-5 PD=1+	04713	244536
40,2	1854-0361	8		TRANSISTOR NPN 2N4239 SI TO-5 PD=800MW	04713	2N4239
V670	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
43-10	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A9 311	1854-0404	0		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
19112	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
49413	1853=0213	7		TRANSISTOR PNP 2N4236 SI TO-5 PD=1W	04713	2N4236
A 9 14 1 4	1854-0361	8		TRANSISTOR NPN 2N4239 SI TO-5 PD=800MW	04713	2N4239
49415	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020

Table 7-3. Replaceable Parts (Part of Change N) (2 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
49416	1854=0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854=0071
A9W17	1854-0404	0		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A9018	1853-0020	4		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853=0020
49019	1853-0213	7		TRANSISTOR PNP 2N4236 SI TO-5 PD=1W	04713	2N4236
05064	1854=0361	8		TRANSISTOR NPN 2N4239 SI TO=5 PD=800Mw	04713	204239
49421 49422	1854-0020	4 7		TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480	1853-0020
74655	1854-0404			TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
49054	1853-0020	0		TRANSISTOR NPN SI TO=18 PD=360MW TRANSISTOR PNP SI PD=300MW FT=150MHZ	28480 28480	1854-0404 1853-0020
49R1	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+=100	24546	C4-1/8-T0-1001-F
49R2	0757-0159	5	8	RESISTOR 1K 1% .5W F TC=0+=100	28480	0757-0159
AGRS	0757-0159	5	~	RESISTOR 1K 1% .5W F TC=0+=100	28480	0757-0159
A9R4	0698-3440	7	4	RESISTOR 196 1% .125W F TC=0+=100	24546	C4-1/8-T0-196R-F
4985	0683-0335	2	5	RESISTOR 3.3 5% .25W FC TC==400/+500	01121	CB33G5
A986	0683-0335	2		RESISTOR 3.3 5% .25W FC TC==400/+500	01121	CB33G5
A9R7	0757-0401	0	8	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-70-101-F
A9R8	0757-0401	0		RESISTOR 100 1% .125W F TC=0+=100	24546	C4-1/8-T0-101-F
49R9 49R10				NOT ASSIGNED NOT ASSIGNED		
A9R11	0757=0280	3		RESISTOR 1K 1% _125W F TC=0++100	24546	C4-1/8+T0=1001=F
49812	0757-0159	5		RESISTOR 1K 1% .5W F TC=0++100	28480	0757-0159
A9R13	0757-0159	15		RESISTOR 1K 1% ,5W F TC=0++100	28480	0757-0159
A9R14	0698-3440	7		RESISTOR 196 1% .125W F TC=0+=100	24546	C4=1/8=T0=196R=F
A9H15	0683-0335	2		RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB33G5
A9R16	0683-0335	2		RESISTOR 3.3 5% .25% FC TC==400/+500	01121	CB33G5
A9R17	0757-0401	0		RESISTOR 100 1% .125W F TC=0++100	24546	C4-1/8-T0-101-F
A9R18	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A9R19 A9R20				NOT ASSIGNED NOT ASSIGNED		
A9R21	0757=0280	3		DEGIGIOD AN AN ANEW E TOWN.	24546	C4-1/8-T0-1001-F
49R22	0757=0159	5		RESISTOR 1K 1% _125W F TC=0+=100 RESISTOR 1K 1% _5W F TC=0+=100	28480	0757-0159
A9R23	0757=0159	5		RESISTOR 1K 1% 5W F TC=0+=100	28480	0757=0159
A9R24	0698-3440	7		RESISTOR 196 1% .125W F TC=0++100	24546	C4-1/8-T0-196R-F
A9R26	0683-0335	5		RESISTOR 3.3 5% ,25W FC TC=-400/+500	01121	C833G5
A9R27	0757-0401	0		RESISTOR 100 1% .125W F TC=0+=100	24546	C4-1/8-T0-101-F
A9R28	0757-0401	0		RESISTOR 100 1% .125W F TC=0+=100	24546	C4-1/8-T0-101-F
A9R29				NOT ASSIGNED		
A9R30 A9R31	0757-0280	3		NOT ASSIGNED RESISTOR 1K 1% _125W F TC=0+=100	24546	C4=1/8=T0=1001=F
A9R32	0757=0159	5			28480	0757=0159
49R33	0757-0159	5		RESISTOR 1K 1% .5w F TC=0+-100 RESISTOR 1K 1% .5w F TC=0+-100	28480	0757=0159
A9R3u	0698=3440	7		RESISTOR 196 1% .125W F TC=0+=100	24546	C4-1/8-T0-196R-F
49R35	0811=2815	6	5	RESISTOR 1.5 5% .75W PW TC=0+=50	91637	RS1/2=T2=1R5=J
A9R36	0811-2815	0		RESISTOR 1.5 5% .75W PW TC=0+=50	91637	R51/2=T2=1R5=J
A9R37	0757-0401	0		RESISTOR 100 1% .125w F TC=0+=100	24546	C4-1/8-T0-101-F
A9R38	0757+0401	0		RESISTOR 100 1% .125W F TC=0+=100	24546	C4=1/8=T0=101=F
AGVR1	1902-3002	3	ц	DIODE=ZNR 2.37V 5% DO=7 PD=.4W TC==.074%	28480	1902=3002
APVRZ	1902=3002	3	7	DIODE-ZNR 2.37V 5X DO-7 PD=.4W TC=+.074X	28480	1902=3002
APVR3	1902-3002	3		DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=074%	28480	1902-3002
49VR4	1902=3002	3		DIODE-ZNR 2.37V 5% DO-7 PD=,4W TC=-,074%	28480	1902-3002
				A9 MISCELLANEOUS		
	1480=0073	6	2	PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU	28480	1480=0073
	4040-0752	9	ž	EXTRACTOR-PC BOARD YEL POLYC	28480	4040=0752

A9 ASSEMBLY

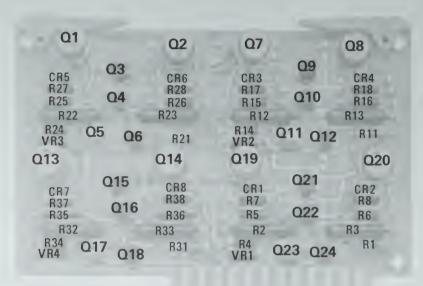


Figure 7-6. A9 Attenuator Driver Assembly Component Locations (Part of Change N)

CHANGE Q

Table 5-1:

Delete the entry for A21R36.

Table 6-3 and Service Sheet 10 (schematic):

Delete A21R36.

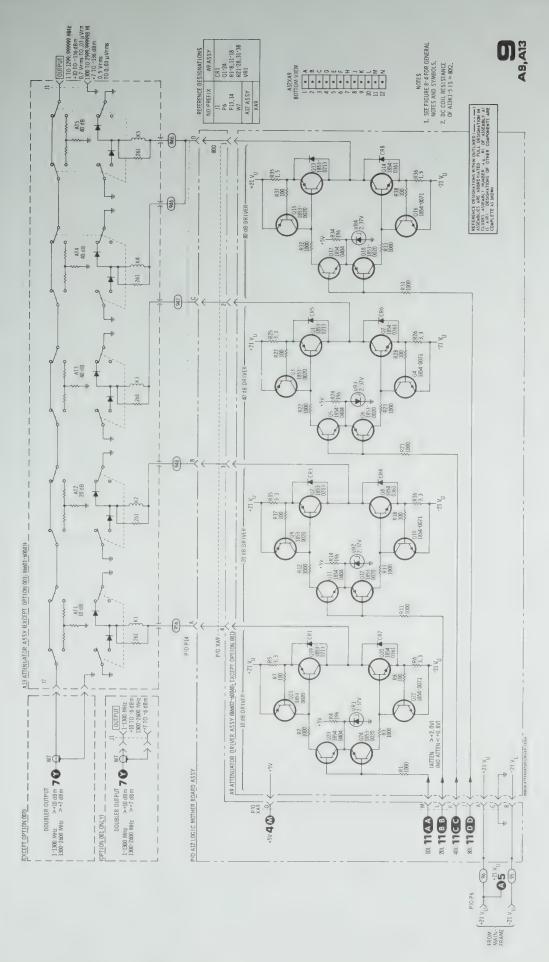
CHANGE R

Table 6-3:

Change A2R9 to 0757-0276 RESISTOR 61.9 1% .125 W F TC = 0 + - 100.

Service Sheet 8 (schematic):

Change the value of A2R9 to 61.9 ohms.





Model 86603A Service

SECTION VIII SERVICE

8-1. INTRODUCTION

- 8-2. This section contains troubleshooting and repair information for the RF Section plug-in. Safety of technical personnel is considered. Circuit operation and troubleshooting on system, plug-in and assembly levels is provided.
- 8-3. The service sheets normally include principles of operation and troubleshooting information, a component location diagram, and a schematic, all of which apply to a specific portion of circuitry within the instrument.
- 8-4. Information related to operation of the RF Section plug-in as part of the 8660-series Synthesized Signal Generator System is provided in Service Sheet 1.
- 8-5. Service Sheets 2 and 3 include an overview of RF Section operation, troubleshooting on an assembly or stage level, and a troubleshooting block diagram. The block diagrams also serve as an index for the remaining service sheets.
- 8-6. The Schematic Diagram Notes, Figure 8-1, aid in interpreting the schematics.
- 8-7. The last foldout in the manual includes a table which cross-references all pictorial and schematic locations of each assembly, chassis mounted component, and adjustable component. The figure is a pictorial representation of the RF Section and shows location of the aforementioned parts.

8-8. SAFETY CONSIDERATIONS

- 8-9. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition (see Sections II, III, and V). Service and adjustments should be performed only by qualified service personnel.
- 8-10. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

8-11. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

WARNING

The service information is often used with power supplied and protective covers removed from the instrument. Energy available at many points may, constitute a shock hazard.

8-12. PRINCIPLES OF OPERATION

- 8-13. The Principles of System Operation explains how the RF Section operates within the Synthesized Signal Generator System, i.e., how other sections affect the RF Section and in turn how they are affected by the RF Section. Control functions in both local and remote modes are also explained.
- 8-14. Service Sheet 1 includes a block diagram and an explanation of system operation with respect to the RF Section.
- 8-15. Overall operation of the RF Section is discussed in Service Sheet 2 and 3. The remaining service sheets are concerned only with sections and/or circuit assemblies within the RF Section plug-in.

8-16. TROUBLESHOOTING

NOTE

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting Guide). Then, if that information indicates possible problems in the RF Section, refer to the Systems Troubleshooting information in Service Sheet 1. This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe. If the problem is in this plug-in, turn to Service Sheet 2 for further troubleshooting information.

8-17. System Troubleshooting

8-18. The System Troubleshooting information in Section VIII of the HP 8660-series mainframe manual should be used when first attempting to isolate a circuit defect. If the defect cannot be isolated to an individual instrument in the system, the technician is normally directed to the System Troubleshooting in the RF Section manual (Service Sheet 1). The problem may then be isolated to the RF Section, Modulation Section, Frequency Extension Module, or the mainframe.

8-19. RF Section Troubleshooting

8-20. When the defect has been isolated to the RF Section, refer to Service Sheet 2. This information is used to isolate the problem to a section or assembly.

8-21. Troubleshooting Aids

- 8-22. Circuit Board Aids. Test points are physically located on the circuit boards as metal posts or circuit pads and usually have either a reference designator (such as TP1) or a label which relates to the function (AM, Pulse, ID, etc.). Transistor emitters, diode cathodes, the positive lead of electrolytic capacitors, and pin 1 of integrated circuits are indicated by a variety of symbols such as E, a diode symbol, +, and a tear-drop shape respectively. Also, a square circuit pad (as opposed to the round pad) may be used in place of any of the previously mentioned symbols.
- 8-23. Service Sheet Aids. RF levels, ac voltages, and dc voltages are often shown on schematic diagrams. Integrated circuit connection diagrams plus diagrams of relays and printed circuit connectors help to locate specific inputs and outputs. Notes are used to explain certain circuits or mechanical configurations not easily shown on the schematic.
- 8-24. The locations of individual components mounted on printed circuit boards are found on individual service sheets on the pictorial representation of the circuit boards. Chassis mounted parts, major assemblies, and adjustable components locations are found on the last foldout in this manual.
- 8-25. Table 8-1, Schematic Diagram Notes, provides information relative to symbols and values shown on the schematic diagrams.

- 8-26. Service Kit and Extender Boards. The HP 11672A Service Kit contains interconnect cables RF cables, various coaxial adaptors, and an adjustment tool, all of which are useful in servicing the RF Section plug-in. Refer to the HP 11672A Operating Note for a listing and pictorial representation of the contents. A list of the service kit contents is also found in the Test Equipment and accessories list in Section I of the mainframe manual.
- 8-27. Circuit board extenders are provided with the mainframe. These extender boards enable the technician to extend plug-in boards clear of the assembly to provide easy access to components and test points. Refer to the list found under Accessories Supplied in Section I of the mainframe manual.

8-28. RECOMMENDED TEST EQUIPMENT

8-29. Table 1-2 lists the test equipment and accessories recommended for use in servicing the instrument. If any of the recommended test equipment is unavailable, instruments with equivalent specifications may be used.

8-30. REPAIR

8-31. General Disassembly Procedures

CAUTION

The Model 86603A RF Section, when used with early model mainframes, has —32 Vdc exposed on the A20 Assembly and on Q1 whenever the mainframe LINE switch is set to STBY. During adjustment and maintenance, do not contact these parts with metal tools. Damage can occur to the mainframe power supply, the A20 Assembly and/or Q1. Models 8660A and 8660C with serial prefixes 1508A and below, and all 8660B's, have this characteristic.

- 8-32. Procedures for removing the RF Section plugin from the mainframe and the covers from the plugin are found on the left-hand foldout page immediately preceding the last foldout in the manual.
- 8-33. The machine screws used throughout the plugin have a Pozidriv head. Pozidriv is very similar in appearance to the Phillips head, but using a Phillips screwdriver may damage the Pozidriv screw head.

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8-34. Non-Repairable Assemblies

8-35. Repairs should not be attempted on the following assemblies if any is found to be defective during troubleshooting:

A5 Modulator Assembly

A6 1-1300 MHz Amplifier Assembly

A8 4 GHz Amplifier Assembly

A13 Attenuator Assembly

A15 20 MHz Amplifier Assembly

A18 Circulator Assembly

A19 3.9 - 4.1 GHz Isolator Assembly

AT1 Isolator

AT2 3 dB Attenuator

FL1 4 GHz Band Pass Filter

NOTE

The A22 Frequency Doubler Assembly is a partially repairable assembly. Refer to the paragraph entitled Repair Procedures for more information.

8-36. Module Exchange Program

8-37. The following restored assemblies may be ordered as replacements under the Module Exchange Program:

A13 Attenuator Assembly
A22 Frequency Doubler Assembly

Refer to Section VI for ordering information.

8-38. Repair Procedures

8-39. LO Signal Circuits Repair Procedure. Refer to Figure 8-1. This procedure is used in conjunction with Service Sheet 2 for isolating circuit defects which are evident as a phase modulation problem

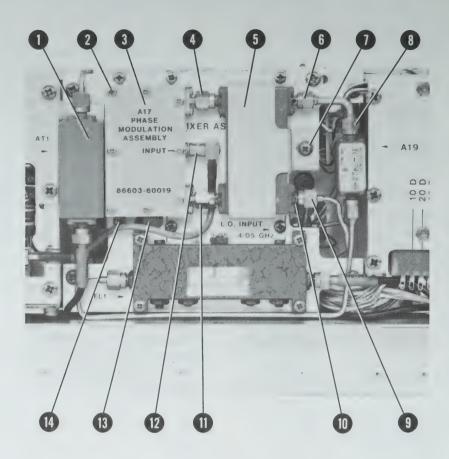
or an incorrect LO signal level (Option 002 instruments only). Perform the procedure if one of the following components is suspected of being defective: W1, W2, W10, W13, W14, A7, A8, A17, A18, A19, or AT2.

- 8-40. The A22 Frequency Doubler Assembly Repair Procedure. Refer to Figure 8-2. This procedure is used after it has been determined that the problem is in the A22A2 Assembly, A22A3 Assembly, or elsewhere in the A22 Assembly. Refer to Service Sheet 7 for A22 Assembly troubleshooting procedures.
- 8-41. Front Panel Housing Disassembly and Repair Procedure. Circuits and parts located in the Front Panel Housing are the meter, output range switch, and vernier control, and (in option 003 instruments) the A23 Doubler Logic Assembly. Perform the procedure in Table 8-1 to gain access to these circuits for purposes of repair.
- 8-42. Rear Panel Disassembly Procedure. To gain access to assemblies and parts mounted on or behind the rear panel, refer to Figure 8-3. The A12 Logic Mother Board, A15 20 MHz Amplifier, Frequency Doubler Test Switch, A24 Frequency Doubler Test Switch Assembly (option 003 only) and the P6 Interconnect Plug are accessible only after removing the panel.

8-43. Post Repair Adjustments

8-44. After a defective circuit is repaired, refer to Section V and perform the adjustment procedure(s) for circuits which *may be affected* by the change. Consider the instructions under paragraphs entitled Related Adjustments and Post Adjustment Tests.

L.O. SIGNAL CIRCUITS REPAIR



NOTE

In conjunction with this procedure, use the troubleshooting information on Service Sheet 2 to isolate a circuit malfunction to one of the following assemblies, circuits, or cables: A7, A8, A18, A19, AT2, W1, W2, W10, or W13 (RF problem); A17 or W14 (phase modulation problem). The procedure applies for option 002 instruments only.

- a. Set the mainframe LINE switch to STBY.
- b. Remove screws 2, 7, and 14 to release the A17 Phase Modulator 3 and A18 Circulator 5 Assemblies.
- c. With a 5/16" open end wrench, loosen the SMA connectors 6, 8, and 9. Carefully pull the assemblies 3 and 5 away from the aluminum decking until A17 3 slips past AT1 1.

Figure 8-1. L.O. Signal Circuits Repair (1 of 3)

- d. Phase Modulation Problems. Separate A17 and A18 at connectors 4 and 11. Set the system LINE switch to ON. Measure the output of W14 at connector 12.
- e. Set the system LINE switch to STBY, replace the defective part of the assembly. Reassemble the items in the reverse order given for disassembly.

CAUTION

Be sure W14 13 runs under connector 11 and is not crushed under A17 7.

- f. RF Problems. To measure the LO signal at the output of A18 10, remove the SMA connectors 6 and 8, and set the System LINE switch to ON.
- g. If the output from A18 is correct, proceed to step h. Otherwise, determine which of A18, W13, A19, or W1 is defective by measuring the outputs of W13, A19, and W1. Refer to Service Sheet 2.

CAUTION

With the LINE switch in the STBY position, the +32 Vdc unregulated voltage may be connected to the RF Section A20 Assembly and Q1. During maintenance, care must be taken not to contact these parts. Damage to the mainframe power supply may occur.

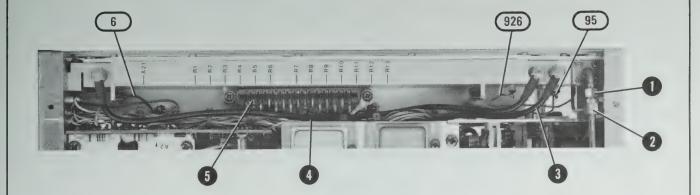
- h. Disconnect the System's line (mains) power. Release the A20 Assembly by removing the screws (one each where circuit board and aluminum decking meet). Lift the assembly straight up. Connect a ground lead from the chassis to the angle bracket which is connected to the ground point on the circuit board.
- i. Remove cable W2 at the A8 Assembly output. (The A8 output jack is closer to the top of the RF Section).
- j. Reconnect the System's line (mains) power. Measure the output level from A8 (refer to Service Sheet 2). If the output level is correct, determine if cable W2 or the A7 Mixer Assembly is defective. If the level is incorrect, proceed to step k.
- k. Remove the three screws which secure the A8 Assembly. Remove the cable connector at the output of A18. Carefully pull A8 away from the decking so the end of AT2 (connected to the input of A8) is exposed.
- 1. With the wrench, loosen and remove AT2 from A8. Carefully remove W10 and AT2 from between the decking.
- m. Reconnect the cable to the output of A18 10. Check the outputs from AT2 and W10 to determine if AT2, W10, or A8 is defective (refer to Service Sheet 2).

n. Discard the defective part or assembly. Reassemble the items removed in the reverse order (leave A20 till last).

CAUTION

When tightening the coaxial connectors, be sure the other end of the cable can be connected without bending the cable. Be sure all connectors are tightened but only enough to ensure a good connection. Excessive bending of semi-rigid coax or excessive tightening of the connectors may damage the cables and/or connectors beyond repair.

FREQUENCY DOUBLER ASSEMBLY REPAIR



If the entire A22 Assembly is to be replaced, proceed as follows:

- a. Disconnect the semi-rigid output cable W7 and the coupler 1. DO NOT attempt to turn the coupler with the 1/4" wrench. Loosen the SMA connector 2 with the 5/16" wrench.
- b. Remove the black cable W16 4 by pulling the slide-on connectors, at each end of the cable, away from the jack.
- c. Remove black cable W15 3 at the input to the A22 Assembly by pulling the slide-on connector away from the jack.
- d. Remove the Pozidriv screws at either end of the A22 Assembly (2 at the rear panel and 2 at the bracket on rear of Front Panel Housing).
- e. Remove the A21 Filter Drive Assembly
- f. Remove the screws which hold the printed circuit board connector 5 in place.
- g. Unsolder the wires to the feed through capacitors. (Wire colors are shown in the illustration).

- h. Refer to Section VI for new or exchange part numbers. For exchange assemblies, DO NOT send the W16 cable in with the casting. BE SURE the covers are included.
- i. To reinstall the A22 Assembly, follow the procedure in the reverse order.

CAUTION

When reinstalling the assembly DO NOT crush any wires between the A13 and A22 Assembly.

If the A22A2 or A22A3 Assemblies are to be replaced, proceed as follows:

a. Remove the six screws which hold circuit board in place.

CAUTIONS

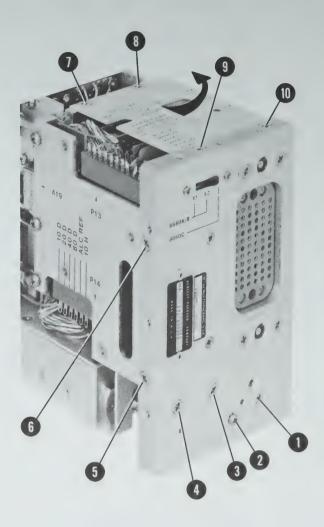
- 1. Do not use flux remover anywhere near the A22 Assembly. The monoblock capacitors may be damaged by this chemical. If absolutely necessary, use only freon or methanol.
- In using a soldering iron to remove the A22A2 or A22A3 Assemblies, care must be taken to avoid damage to the transistors, diodes, and monoblock capacitors, some of which are extremely heat sensitive.
- b. Unsolder the input and output connections to the board being replaced on the adjacent circuit boards.
- c. If replacing the A22A3 circuit board, unsolder the +24 Vdc power supply connection from the feedthrough capacitor.
- d. On the board being replaced, unsolder the resistor which is connected to the other amplifier circuit board.
- e. Lift the circuit board straight up and out of its cavity.
- f. Unsolder the input and output wire connectors. Be sure to save the plastic insulators.
- g. To install the circuit board, follow the preceding steps in the reverse order except solder the input and output wire connectors into place after putting the board into the cavity and installing the six screws.

Table 8-1. Front Panel Housing Repair

FRONT PANEL HOUSING DISASSEMBLY AND REPAIR

- a. Place the RF Section in the normal upright position.
- b. With a Pozidriv screwdriver, remove the two screws which hold the top of the front panel to the housing.
- c. Turn the plug-in over with the bottom up. Remove the screw which is seen through the curved cutout slot in the latch when it is in the closed or latched position.
- d. With a knurled nut wrench, loosen the knurled nut on the OUTPUT jack. Remove the nut by hand.
- e. Pull the front panel away from the housing.
- f. Determine what part or assembly is defective and replace it.
- g. Reinstall the front panel by followint the preceding steps in the reverse order. Be careful not to crush any wires between the front panel and the chassis.

REAR PANEL DISASSEMBLY



- a. On the rear panel, remove the screws 1 and 2 which hold the A22 Assembly in place.
- b. Remove the screws 3 and 4 which hold the A13 Assembly in place.
- c. Remove the screws **9** and **10** which hold the top rear deck to the rear panel.
- d. In Option 003 instruments, remove the two screws 7 and 8 which hold the top rear deck to the bulkhead.

Figure 8-3. Rear Panel Disassembly (1 of 2)

CAUTION

To avoid damage to the rear panel switch, carefully slide the deck to the right while twisting it just enough to bring it out from under the rear panel lip. DO NOT FORCE the deck out.

e. Remove the screws 5 and 6 which hold the rear panel to the left rear deck. Carefully pull the rear panel back and away to expose the assemblies and parts.

SCHEMATIC DIAGRAM NOTES Resistance in ohms, capacitance in microfarads, inductance in microhenries unless otherwise noted. Asterisk denotes a factory-selected value. Value shown is typical. Part might be omitted. See Table 5-1. Indicates backdating. Refer to Table 7-2. Tool-aided adjustment. Manual control. Encloses front-panel designation. Encloses rear-panel designation. Circuit assembly borderline. Other assembly borderline. Also used to indicate mechanical interconnection (ganging). Heavy line with arrows indicates path and direction of main signal. Heavy dashed line with arrows indicates path and direction of main feedback. Wiper moves toward CW with clockwise rotation of control (as viewed from shaft or knob). Numbered Test Lettered Test point. No measurement point. Measureaid provided. ment aid provided. Encloses wire color code. Code used is the same as the resistor color code. First number identifies the base color, second number identifies the wider strip, third number identifies the narrower stripe. E.g., (947) denotes white base, yellow wide stripe, violet narrow stripe. A direct conducting connection to the earth or a structure that has a similar function (e.g., the frame of an air, sea, or land vehicle). or a conducting connection to a chassis or frame. Coaxial or shielded cable. Stripline (i.e., RF transmission line above ground).

Figure 8-4. Schematic Diagram Notes (1 of 3)

SCHEMATIC DIAGRAM NOTES



Arrows on relays indicate direction of arm movement when energized.



Filters. Specific type indicated by crosses on curved lines.



Example of Highpass Filter.

SWITCH DESIGNATIONS

EXAMPLE: A3S1AR(2-1/2)

A3S1 = SWITCH S1 WITHIN ASSEMBLY A3

> A = 1ST WAFER FROM FRONT (A=1ST, ETC)

R = REAR OF WAFER (F=FRONT)

(2-1/2) = TERMINAL LOCATION (2-1/2) (VIEWED FROM FRONT)

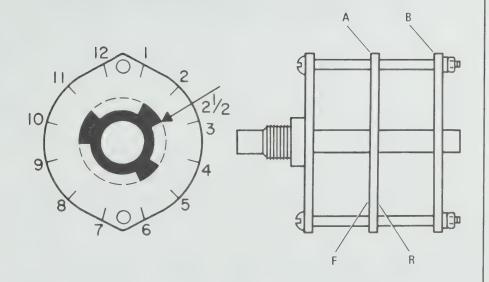


Figure 8-4. Schematic Diagram Notes (2 of 3)

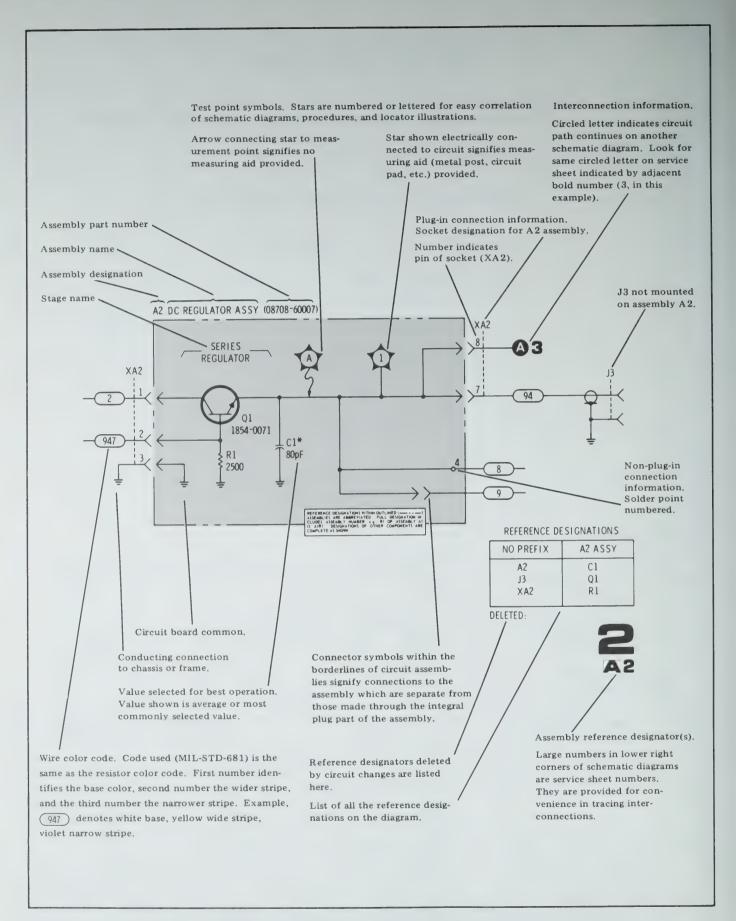


Figure 8-4. Schematic Diagram Notes (3 of 3)

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SERVICE SHEET 1

NOTE

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting Guide). Then, if that information indicates possible problems in the RF Section, refer to the Systems Troubleshooting information in this manual (Service Sheet 1). This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe. If the problem is in this plug-in, refer to Service Sheet 2 for further troubleshooting information.

RF SECTION OPERATION IN THE SYNTHE-SIZED SIGNAL GENERATOR SYSTEM

In order to understand the operation of the RF Section or to effectively troubleshoot it, the entire Synthesizer Signal Generator System must be understood. The emphasis here is on the RF Section and its relationship with the other units which make up the system.

PRINCIPLES OF OPERATION

The HP Model 86603A RF Section plug-in (as part of the HP 8660-series Synthesized Signal Generator System) has an RF Output of +7 to -136 dBm across 50Ω from 1 to 2599.999998 MHz. The RF signals coupled from mainframe to the Frequency Extension Module are converted to two phase-locked outputs which are coupled to the RF Section. The signals are mixed, amplified, and coupled to the OUTPUT jack through the RF Attenuator.

The RF detector produces a dc output proportional to the RF output signal. The dc output is compared to a reference voltage. Any difference in dc levels produces an error current which drives the PIN diode modulator. The current flow through the PIN diodes controls the RF output level. The negative feedback loop described, is an ALC loop which holds the RF output level constant.

Output Frequency Selection

The desired output frequency is selected by the Digital Control Unit (DCU) in the mainframe. Control logic levels to the mainframe RF circuits set the frequencies of the signals to the Frequency

Extension Module. Other logic levels are coupled to the extension module from the mainframe to set the frequency of the generated RF outputs which are coupled to RF Section. The signals are mixed and the converted signal is coupled to the Frequency Doubler. In the X1 mode (<1300 MHz) the signal is passed directly to the RF Attenuator and on to the OUTPUT jack. In the X2 mode, the converted signal frequency is doubled before being input to the RF Attenuator.

Modulation Selection

Depending on the Auxiliary or Modulation Section, amplitude, frequency, phase, or pulse modulation may be selected.

NOTE

In the FM and ϕM modes, frequency and phase deviation is doubled in the Frequency Doubler Assembly at center frequencies ≥ 1300 MHz (X2 mode).

- a. The amplitude modulation drive signal is coupled to the RF Section from the Modulation Section. The drive signal is superimposed on the reference level which controls the ALC loop. Thus, the ALC loop causes the RF output level to change at the modulation signal rate.
- b. Frequency modulation is accomplished by setting the modulation mode control to FM. The modulation drive signal frequency modulates a 20 MHz VCO signal which is generated in the Modulation Section. This signal is coupled to the RF Section, amplified, and coupled on to the Frequency Extension Module. The extension module circuits transfer the frequency modulation information from the 20 MHz signal to the 3.95 to 2.75 GHz oscillator signal. This signal is then coupled to the RF Section circuits.
- c. Phase modulation occurs when the selected modulation mode is set to ϕM . The modulation drive signal from the modulation section is applied to the LO signal so its phase deviation varies with the drive signal amplitude.
- d. The Pulse ID logic input opens the ALC loop so there is no RF output without a pulse modulation drive signal. A -10 volt peak pulse will momentarily bias the RF output on.

SERVICE SHEET 1 (Cont'd)

RF Output Level Selection

The RF output level is selected by the front panel OUTPUT RANGE switch and the VERNIER control. The VERNIER control (in conjunction with the front panel meter) is used to set the output within a usable range of 10 dB. The OUTPUT RANGE switch controls the output level range by inserting attenuation in 10 dB steps to 140 dB.

Remote Operation

In remote mode the frequency, modulation, and RF output levels are programmed into the DCU. Through parallel BCD PI (plug-in) control lines, an input is sent to the various storage registers. A one-of-six address selects the register which will accept the information. Frequency information is routed into one of 3 registers: center frequency, step (except 8660A), and sweep (except 8660A). Modulation information is routed to either the Modulation Mode/Source register or the Modulation Level register. RF output level (attenuation) information is routed to the attenuation storage register in the RF Section by addressing the ATTN CLK.

The attenuation information is stored in the register until new data is received. Until that time the stored information is connected through various logic and decoding circuits and applied to the relays and switches which set the RF output level to the desired value. The RF Section front panel controls are inoperative in the remote mode.

SYSTEM TROUBLESHOOTING

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting Guide). Then, if that information indicates possible problems in the RF Section, return to this service sheet and perform the following tests which may help isolate the problem to an instrument (mainframe or a plug-in).

Preparing the RF Section for Troubleshooting

Follow the Removal and Disassembly Procedures on the foldout page which just preceeds the last foldout in the manual. Follow the directions for removing the RF Section from mainframe, removing its covers, and making the interconnections from mainframe to RF Section for troubleshooting purposes.

Output Level Incorrect

The following steps check the signal levels input to the RF Section from the Frequency Extension Module. Also, the attenuation data input to the RF Section must be checked if the instrument is being operated in the remote mode.

Model 86603A

- a. Disconnect the RF cable connected to P2 (on rear panel below the multi-pin connector P6). Measure the level of the 3.95 to 2.75 GHz signal from the cable with a spectrum analyzer (>+10 dBm). Reconnect the cable to P2.
- b. Disconnect the RF cable connected to P1 (on rear panel below the multi-pin connector). Measure the level of the 3.95 to 4.05 GHz signal from the cable with a spectrum analyzer (>-6 dBm). Reconnect the cable to P1.
- c. If either signal level from the extension module is incorrect, the problem is either in the extension module or the interconnections to the RF Section. Check the continuity of the cables and, if necessary, refer to the extension module manual for further troubleshooting information.
- d. If both signal levels are correct and the system is being operated in the remote mode, switch to local (front panel) control. If the problem is still evident, refer to Service Sheet 2 for further troubleshooting information.
- e. If the problem disappears, check continuity of the input data lines (PI-1, PI-2, PI-4, and PI-8) and the ATTN CLK input to the mainframe. If continuity exists, proceed to Section VIII of the mainframe manual and troubleshoot the DCU. Otherwise, refer to Service Sheet 3.

Frequency Problems

The mainframe center frequency readout is correct but the frequency at the RF Section's front panel jack is incorrect. The mainframe, extension module, and RF Section have controlled frequency sections. [If the problem is related to frequency doubling mode (≥1300 MHz), the problem is in the RF Section or DBL-L input from the mainframe (proceed to step d).] If the RF frequencies to the extension module are incorrect or the levels are low, the circuit defect is in the mainframe or the RF Section interconnections to the extension module (including the A15 20 MHz Amplifier

Model 86603A Service

SERVICE SHEET 1 (Cont'd)

Assembly). If these levels and frequencies are all correct, the extension module is malfunctioning or the data input from the mainframe DCU is incorrect.

NOTE

If coaxial test cable 11672-60008 (for checking outputs from the multi-pin connector J6) is not available, proceed to step b.

- a. Check the low frequency RF inputs to the RF Section. Set the mainframe Line switch to standby (STBY), disconnect the interconnect cable from the multi-pin connector P6 on the RF Section rear panel. Return the mainframe line switch to the ON position. Check the frequencies and levels according to the tables with a Spectrum Analyzer and a frequency counter. If the levels and frequencies are all correct, the same signals must be checked to ensure continuity into the Frequency Extension Module. Refer to the Troubleshooting Information in the extension module manual. Otherwise, proceed to step b.
- b. Check the RF signal levels and frequencies at their assembly outputs in the mainframe. Refer to the Section VIII of the mainframe manual. Check the 20 MHz FM/CW signal at A4J7, 100 MHz at A4J8, and 360 to 450 MHz at A4J12. The 20 to 30 MHz signal is found on the A2 Mother Board Assembly which is located directly beneath the A4 Assembly. The tables of levels and frequencies still apply for these measurements. If any of the outputs are incorrect, refer to the appropriate troubleshooting information relating to the circuits which generate that particular frequency in Section VIII of the mainframe manual.
- c. If all inputs (step b) are correct and if any of the J6 outputs (step a) were incorrect, check continuity of the interconnections to the RF Section. In the case of problems with the 20 MHz CW/FM signal, refer to the Modulation Section manual. If all inputs (step b) are correct and the J6 outputs to the RF Section were not checked, proceed to the extension module for further troubleshooting information.

NOTE

If the problem is not in the RF Section or interconnections, the information in

the Frequency Extension Module will determine if the problem is in the digit 8, 9, and 10 logic control inputs from the mainframe or the frequency controlled circuits in the extension module.

d. If the problem is related to frequency doubling, be sure the rear panel Frequency Doubler Test Switch is in the proper position. Then recheck for correct operation.

NOTE

The test switch normally will be set to the 8660C position. If the RF Section is being tested for proper operation in either a Model 8660A or 8660B mainframe, the switch should be in either the X1 or X2 position depending on which mode seems to be defective.

CAUTION

Model 8660A and 8660B mainframes of serial prefix 1349A and below must be modified before RF Sections can be used in the X2 frequency mode or if the RF Section has the phase modulation capability. Refer to the paragraph entitled Modifications in Section II.

e. If necessary, change the test switch position and insert the RF Section into another mainframe. If another mainframe is not available, proceed to step g.

RF Signal Levels

Pin Numbers J6 (Main- frame) or Inter- connect Cable	Frequency* (MHz)	Signal Level (dBm)
62	20 MHz ± 1 Hz	>-7 dBm
63	20 to 30 MHz ± 1 Hz	>-7 dBm
64	360 to 450 MHz ± 1 Hz	>+10 dBm
65	>+10 dBm	

*To achieve the ± 1 Hz tolerance, the System mainframe and the frequency counter must share a common timebase.

Center Frequency Versus Frequency of 20 to 30 MHz Signal*

Center Frequency Readout (MHz)	Exact Frequency (20 to 30 MHz Signal) (MHz)	Center Frequency Readout (MHz)	Exact Frequency (20 to 30 MHz Signal) (MHz)	Center Frequency Readout (MHz)	Exact Frequency (20 to 30 MHz Signal) (MHz)		
0.000000	30.000000	0.000400	29.999600	0.080000	29.920000		
0.000001	29.999999	0.000500	29.999500	0.090000	29.910000		
0.000002	29.999998	0.000600	29.999400	0.100000	29.900000		
0.000003	29.999997	0.000700	29.999300	0.200000	29.800000		
0.000004	29.999996	0.000800	29.999200	0.300000	29.700000		
0.000005	29.999995	0.000900	29.999100	0.400000	29.600000		
0.000006	29.999994	0.001000	29.999000	0.500000	29.500000		
0.000007	29.999993	0.002000	29.998000	0.600000	29.400000		
0.000008	29.999992	0.003000	29.997000	0.700000	29.300000		
0.000009	29.999991	0.004000	29.996000	0.800000	29.200000		
0.000010	29.999990	0.005000	29.995000	0.900000	29.100000		
0.000020	29.999980	0.006000	29.994000	1.000000	29.000000		
0.000030	29.999970	0.007000	29.993000	2.000000	28.000000		
0.000040	29.999960	0.008000	19.992000	3.000000	27.000000		
0.000050	29.999950	0.009000	29.991000	4.000000	26.000000		
0.000060	29.999940	0.010000	29.990000	5.000000	25.000000		
0.000070	29.999930	0.020000	29.980000	6.000000	24.000000		
0.000080	29.999920	0.030000	29.970000	7.000000	23.000000		
0.000090	29.999910	0.040000	29.960000	8.000000	22.000000		
0.000100	29.999900	0.050000	29.950000	9.000000	21.000000		
0.000200	29.999800	0.060000	29.940000	9.999999	20.000001		
0.000300	29.999700	0.070000	29.930000				

^{*}This table does not contain all possible frequency steps.

f. If the RF Section works properly in the new mainframe, refer to Section VIII of the mainframe manual and troubleshoot the original mainframe. If the RF Section is at fault, proceed to Service Sheet 2.

g. Check the DBL-L input to the RF Section at J6 pin 36. If the input is correct, proceed to Service Sheet 2 for further troubleshooting information. Otherwise, turn to Section VIII of the mainframe manual and troubleshoot the DCU (Digital Control Unit).

Model 86603A Service

SERVICE SHEET 1 (Cont'd)

Center Frequency Versus Frequency of 360 to 450 MHz Signal

Center Frequency	Actual Frequency
Readout	(350 to 450 MHz Signal)
0.00 GHz	450 MHz
0.01	440
0.02	430
0.03	420
0.04	410
0.05	400
0.06	390
0.07	380
0.08	370
0.09	360
0.10	350

Modulation Problems

Amplitude, Frequency, and Phase Modulation. Defects in modulation circuits can usually be classed as either accuracy or distortion problems. In each case it must be determined if the problem is in the Modulation Section, RF Section, or (in FM mode only), the Frequency Extension Module.

a. System modulation accuracy is checked by performing the appropriate performance test in Section IV of the modulation section manual. If the results indicate a problem exists, check the modulation section output with a full scale level setting. The table indicates where to make the measurement, the type of measurement, and the normal signal measured. A coaxial cable from the 11672A Service Kit, the 11672-60008 is used to interconnect the signal from the J6 (the mainframe-to-RF Section interconnect jack).

If the measured signal shows the output modulation signal is incorrect, perform the appropriate adjustment in Section V of the modulation section manual. If the signal cannot be properly adjusted, refer to Section VIII of the modulation section manual for further troubleshooting information. Once the adjustment is satisfactorily made, recheck the system modulation accuracy.

If the system accuracy is still incorrect, perform the appropriate adjustment procedure in Section V of the RF Section manual. If this adjustment cannot satisfactorily be made, refer to the troubleshooting information of Service Sheet 2.

b. Modulation distortion problems are verified by performing the appropriate distortion test determined by the modulation type (refer to Section IV of this manual). If the test indicates an excessive distortion level is present in the RF output signal, the source must be determined.

Measurements of the signals from the Modulation Section may be made at the J6 connector after the RF Section has been removed. For each modulation type, the output distortion is typically <1%. If the distortion is excessive, refer to the trouble-

Modulation Accuracy Test Levels

Modulation Type	Measurement Location	Signal Parameter Measured	Measured Signal (for Full Scale) Modulation Level
Amplitude ¹	A12 Assembly at test point labeled AM. (Right side rear of plug-in or J6 pin 55.	AC Voltage	2.8 Vp-p (1.0 Vrms) at 1 kHz rate
Frequency ²	Pin 62 of J6	Frequency Deviation (peak)	20 MHz ±10 kHz (FM x 1 range) at 1 kHz rate
Phase ¹	A16 Assembly input (white/ green cable) or J6 pin 59	AC Voltage	4.2 Vp-p (1.5 Vrms) at 1 kHz rate

¹ If the input is very low or non-existant, verify that continuity of the input exists back to the modulation section. If continuity exists, refer to Service Sheet 2.

² If no frequency modulation of the RF Signal is present or if the RF signal is incorrect only in the FM mode, refer to Section VIII of the modulation section manual for further troubleshooting information.

SERVICE SHEET 1 (Cont'd)

shooting information in Section VIII of the modulation section manual. Otherwise, perform the appropriate adjustment procedures in Section V of the RF Section manual.

Recheck the performance test in Section IV of this manual. If necessary, refer to the troubleshooting information in Service Sheet 2.

Unusual Phase Modulation Level Problems. If phase modulation level accuracy varies excessively with system center frequency, check the gain tracking inputs (Digit 8) for the correct logic level for the selected center frequency. If the logic levels are incorrect, refer to the mainframe manual for further troubleshooting information. If the inputs are correct, refer to Service Sheet 2.

Pulse Modulation Problems. Pulse Modulation of the Signal Generator System is accomplished by using the HP Model 86631B Auxiliary Section and an external pulse generator.

- a. Set the Auxiliary Section external modulation control to Pulse. To the input jack couple an external pulse of -10 Vpk with the "pulse off" voltage set to 0 Vdc.
- b. Measure the voltage on the test point labeled PULSE (located on a circuit board at the right side rear of the plug-in). This voltage should be about +5 Vdc. Also, check the pulse input from the white-green cable where it enters the A2 Assembly. If either the signal or dc voltage is not present, check continuity back to the Auxiliary Section. If necessary, refer to the HP Model 86631B Operating Note and troubleshoot the Auxiliary Section. Otherwise, refer to Service Sheet 2 for more troubleshooting information.

SERVICE S

When 8660-s shootir indicat Troubl inform plug-in service

ANALOG C

PRINCIPLE

General

The LO and difference is Frequency jack, or to a the harmon frequencies

The RF ou resultant er through the maintains t range.

The RF our remotely cocoupled to attenuation Attenuators

A power su Section. Th Extension N

Phase Modu

The phase r Phase Modu (frequency change in s circuitry ch coupled to t

Phase modu Circulator / circulator. ' dependent modulator. port 2 (J2)

SERVICE SHEET 2 (Cont'd)

Driver Assembly is a distorted sinusoidal waveform of approximately 7.5 Vp-p for a full scale Modulation Section meter indication. If the output is incorrect, check the output of the cable, W12, to determine if W12 or A16 is defective. The output should be 1.5 Vrms. If the output of the A16 assembly is correct, either W14 or A17 is defective. Refer to the paragraph entitled L.O. Signal Circuits Repair procedure in Section VIII of this manual for disassembly and repair procedures.

Phase modulation distortion problems in the RF section will generally be caused by the A16 Phase Modulator Driver Assembly or the A17 Phase Modulator Assembly. Refer to Service Sheet 5.

NOTE

Excessive incidental AM during phase modulation may be caused by incorrect operation of the 50 MHz Low Pass Filter. Check the control input and the RF output level of the filter, Refer to Service Sheet 4.

- g. Pulse Modulation. Problems may be isolated by checking Pulse In and Pulse ID inputs. Also, check continuity from A5 Modulator Assembly inputs from Auxiliary Section.
 - h. Incorrect Front Panel Meter Reading. Refer to Test 3.
- Test 3. If the RF output level is incorrect by more than 1 or 2 dB, proceed to Test 4. Otherwise check the 10H input to the A10 Assembly related components. Refer to Service Sheet 3 if the input is incorrect. If necessary, refer to Section V and perform the RF Output Level and 1 dB Step Attenuator Adjustment procedures. If the Adjustments cannot be done or do not correct the tracking across the VERNIER range, check the Meter Driver and Meter circuitry, and the AM Gain circuits. Refer to Service Sheets 6 and 8 respectively. Also check the circuits in the A4 Assembly which are influenced by the 10H input.
- **Test 4.** Proceed to Test 5 if the RF output level is higher than normal. The RF outputs listed in each step of this test (4) are lower than normal. The three voltages shown in parentheses are Modulator Bias Signal ranges. They indicate that the ALC loop (1) is holding the RF output low, (2) is trying to increase the RF output or (3) that a quiescent level, although incorrect, has been reached. Refer to the block diagram for the normal range of Modulator Bias Signal levels.
- a. The RF output is low but the ALC loop is trying to increase the level (>-3 Vdc). Check the RF outputs of FL1, A7, A6, and A22 to isolate the problem to Service Sheet 4 (for other than option 002 instruments), Service Sheets 4 or 5 (option 002 instruments only), Service Sheet 6, or Service Sheet 7 respectively.

If the output of FL1 is correct and the output of A7 is incorrect, the

Service

SERVICE SHEET 1 (Cont'd)

shooting information in Section VIII of the modulation section manual. Otherwise, perform the appropriate adjustment procedures in Section V of the RF Section manual.

Recheck the performance test in Section IV of this manual. If necessary, refer to the troubleshooting information in Service Sheet 2.

Unusual Phase Modulation Level Problems. If phase modulation level accuracy varies excessively with system center frequency, check the gain tracking inputs (Digit 8) for the correct logic level for the selected center frequency. If the logic levels are incorrect, refer to the mainframe manual for further troubleshooting information. If the inputs are correct, refer to Service Sheet 2.

Pulse Modulation Problems. Pulse Modulation of the Signal Generator System is accomplished by using the HP Model 86631B Auxiliary Section and an external pulse generator.

- a. Set the Auxiliary Section external modulation control to Pulse. To the input jack couple an external pulse of -10 Vpk with the "pulse off" voltage set to 0 Vdc.
- b. Measure the voltage on the test point labeled PULSE (located on a circuit board at the right side rear of the plug-in). This voltage should be about +5 Vdc. Also, check the pulse input from the white-green cable where it enters the A2 Assembly. If either the signal or dc voltage is not present, check continuity back to the Auxiliary Section. If necessary, refer to the HP Model 86631B Operating Note and troubleshoot the Auxiliary Section. Otherwise, refer to Service Sheet 2 for more troubleshooting information.

MAINFRAME INTERCONNECT JACK

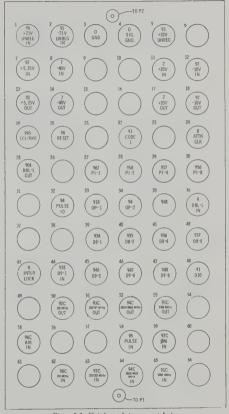
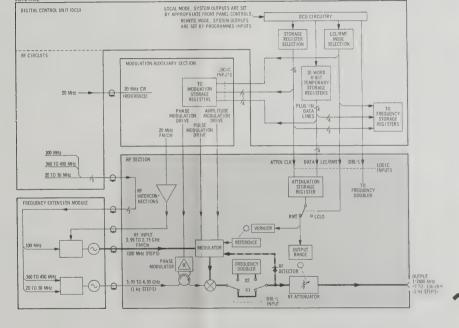


Figure 8-6. Mainframe Interconnect Jack

RF SECTION TEST POINTS RIGHT SIDE VIEW AM PULSE A12 ASSY TEST POINTS LEFT SIDE VIEW PHASE MODULATION PULSE MODULATION INPUT TO THE A16 ASSEMBLY A2 ASSEMBLY

Figure 8-5. System Test Point Locations



DIGITAL CONTROL UNIT (DCU)

Figure 8-7. System Troubleshooting Block Diagram

SERVICE SHEET 2 (Cont'd)

problem may be on either Service Sheets 4 or 5 in option 002 instruments. In this case, refer to the LO Signal Circuits Repair procedure and the Troubleshooting Block Diagram to isolate the problem to an assembly or cable.

On instruments other than option 002 instruments, if the output of A7 is defective, refer to Service Sheet 4.

Each of these assemblies and circuits, if defective, must be replaced as a unit with the exception of A7. If A7 is defective, refer to Service Sheet 4 for further troubleshooting information.

b. The RF output is low and the ALC loop is holding the Modulator Bias Signal level low (>+10 Vdc). First, check the A10 Reference Assembly output with the VERNIER control set to the CW and CCW position with A4S1 in the Normal position. If the output is abnormal, refer to the troubleshooting information on Service Sheet 8. A normal output indicates the defect is either on the A3 ALC Assembly, A22 Frequency Doubler Assembly, or the A4 Detector Amplifier Assembly.

Set the A4S1 switch to the Test position. If the Modulator Bias Signal exhibits the same response as shown in the following table, the problem is either in the A22 Frequency Doubler Assembly which contains the detector or the A4 Detector Amplifier Assembly. (Check the Detector Signal input at A4 pin 11.) Otherwise, Service Sheet 8 contains the necessary troubleshooting information.

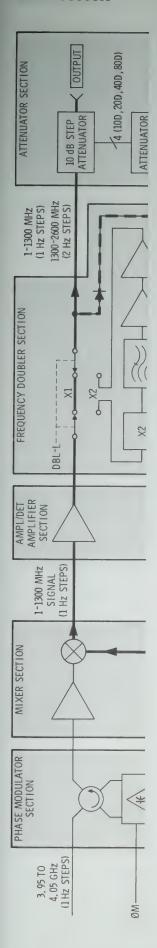
Modulator Bias Signal

A4S1		Vernier Control Settings												
Switch		С	W		CCW									
	90)4	90	7	90)4	907							
Normal	+0.2	Vdc	+0.4	Vdc	+1 to Vo		+0.8	Vdc						
Test	-4	Vdc	-3.0	Vdc	+0.3	Vdc	+0.5	Vdc						

c. The Modulator Bias Signal is at a quiescent level but is lower (more positive) than normal. Check the A10 Reference Assembly output level.

If the output is lower (more positive than normal), check the 1A, 2A, 4A, and 8A inputs to the A10 Assembly (remote mode only). If they are correct or the instrument is in local mode, refer to Service Sheet 8. If the remote inputs are incorrect or the problem is associated with the 10 dB Step Attenuator, refer to troubleshooting information on Service Sheet 3. Otherwise, check the detector output and reference at A4 pin 10 and 11. Refer to either Service Sheet 6 or 7.

- Test 5. The RF outputs listed in each step of this test are higher than normal. The voltages enclosed in parentheses are Modulator Bias Signal ranges. They indicate that the ALC loop (1) is holding the RF output high, (2) is trying to decrease the output level or (3) that a quiescent level, although incorrect, has been reached. Refer to the block diagram for normal values of Modulator Bias Signal.
- a. High RF output level; the ALC has increased the level (≥-3 Vdc). Check the A10 Reference Assembly output. If the response to VERNIER control settings is abnormal, refer to Service Sheet 8 and troubleshoot the A10 Assembly. If the response is normal, set the A4S1 switch to test. If the Modulator Bias Signal responds to the VERNIER control settings as indicated by the table of Test 4b, check that the detector output responds properly to the increased RF signal level (check A4 pin 10 and 11) and refer to either Service Sheet 6 or 7. Otherwise, turn to Service Sheet 8 and continue troubleshooting.
- b. High RF output level; the ALC is trying to decrease the level (>+10 Vdc). The A5 Modulator Assembly or associated circuitry is probably defective (refer to Service Sheet 4).
- c. The Modulator Bias Signal is at a quiescent level but higher (more negative) than normal. Check the A10 Reference Assembly output. If the A10 output is more negative than normal, check the 1A, 2A, 4A, and 8A inputs to the A10 assembly (remote mode only). If the A10 outputs are correct or the instrument is in local mode, refer to Service sheet 8. If the remote inputs are incorrect or the problem is associated with the 10 dB Step Attenuator, refer to the troubleshooting information on Service Sheet 3. Otherwise, check that the detector output responds properly to the increased RF signal level (check A4 pins 10 and 11). Refer to either Service Sheet 6 or 7.



SERVICE SHEET 3 (Cont'd)

to the Logic Assembly. The ATTN CLK controls the data inputs on the PI-1, PI-2, PI-4, and PI-8 lines to the Logic Assembly. The OUTPUTS to the 10 dB Step Attenuator (10L, 20L, 40L, 80L), the over-range (10H), and the 1 dB Step Attenuator outputs (1A, 2A, 4A, 8A) are all controlled by external programming in the Remote Mode. A safety feature, the RESET input, sets the 10 dB Step Attenuator to the maximum attenuation when the Remote mode of operation is first initiated.

Attenuator Driver Assembly

The inputs from the Logic Assembly (10L, 20L, 40L, and 80L) switch the equivalent attenuator drive outputs (10D, 20D, 40D, and 80D). These outputs provide the higher voltages and current needed to drive the relays in the Attenuator Assembly.

Doubler Power Supply Assembly

This assembly provides three outputs which are selected by two inputs from the mainframe. The inputs are set by the system center frequency. At ≥1300 MHz (X2 range), the Doubler Power Supply output connects the +22 Vdc to two RF amplifiers in the Frequency Doubler Assembly. Also, at or above 1300 MHz, +12 Vdc is connected to a relay in the Frequency Doubler Assembly. The Bandwidth Control is switched at center frequencies of 10 MHz or 1300 MHz.

Option 003 Instruments

In option 003 instruments, the A23 Doubler Logic and A24 Frequency Doubler Test Switch Assemblies are added. These circuits allow front panel selection of the frequency range (X1 and X2) when the RF Section is used with 8660A or 8660B mainframes.

TROUBLESHOOTING

Malfunctions in the RF Section which appear to be a logic problem may be an analog circuit problem. Refer to Service Sheet 2 to begin troubleshooting.

Test Equipment

General

If the malfunction is isolated to the logic circuits, the related inputs must be checked before an attempt is made to troubleshoot the individual circuit assemblies. The control levels are fixed and may change when a new center frequency or mode of operation (local or remote) has been selected. The clocked or momentary inputs, PI (plug-in), ATTN CLK, and RESET occur only at the instant the center frequency or mode change is made.

ANALOG CIRCUITS

PRINCIPLES OF OPERATION

General

The LO and RF input signals from the frequency Extension Module are mixed and the difference frequency output (1 to 1300 MHz) is amplified and coupled to the Frequency Doubler Assembly. The signal is either coupled directly to the OUTPUT jack, or to a frequency doubler circuit and tracking bandpass filter. In the latter case, the harmonic signal is amplified before being coupled to the OUTPUT tack. Thus, frequencies between 1 and 2600 MHz may be selected.

The RF output voltage level is sampled and compared to a stable reference. The With desired center frequencies less than 1300 MHz, the Frequency resultant error voltage is used to control the level of the RF signal as it is passed through the Modulator assembly. Therefore, this ALC (Automatic Level Control) loop maintains the output level relatively constant across the system's specified output input frequency to the doubler is exactly half the selected center

The RF output level may be either locally controlled (front panel operation) or remotely controlled (programmed input). In either case, the logic control input is coupled to the Logic Section. This input data is manipulated so it selects the level of Amplifier/Detector Amplifier Section attenuation of the RF output signal by controlling the 10 and/or 1 dB Step Attenuators.

A power supply, RF interconnections, and a 20 MHz amplifier are contained in the RF Section. They supply the power and RF signals which operate the Frequency

Phase Modulator Section

The phase modulation drive signal from the Modulation section is coupled to the A16 Phase Modulation Driver Assembly where it passes through a gain tracking circuit (frequency variable attenuator). This circuit keeps the modulation level constant with change in system center frequency because the sensitivity of the phase modulator circuitry changes with respect to the LO frequency. The signal is then amplified and

Phase modulation of the LO signal occurs when the signal (which passes through the Circulator Assembly to the Phase Modulator Assembly) is reflected back into the circulator. The phase of the reflected signal with respect to the incident signal is In the AM mode the modulation drive signal is superimposed on the dependent on the instantaneous modulation drive voltage present at the phase reference voltage. The average amplitude of the RF output is modulator. The LO signal is first passed through the isolator, through port 1 (J1) to dependent on the average dc level (which is equal to the dc reference port 2 (J2) of the circulator, and on to the phase modulator. The reflected signal is voltage) while the instantaneous RF output voltage and its rate of

SERVICE SHEET 2 (Cont'd)

passed from port 2 to port 3 (J3) where it is again reflected from the phase modulator with additional phase shift approximately equal to that which occurred at port 2. The signal is passed from port 3 to port 4 (J4) and through the 3 dB attenuator to the 4 GHz Amplifier Assembly.

In other than option 002 instruments (no phase modulation circuits). the LO signal is coupled directly from FL1 to the A8 4.0 GHz Amplifier Assembly

Mixer Section

The mixer output is derived from mixing the LO and RF inputs. The phase modulated or cw LO signal is amplified and coupled to the Mixer Assembly. The RF signal passes through the Isolator (20 dB reverse isolation) to the Modulator Assembly where it encounters variable series attenuation. The series attenuation is controlled by the bias signal from the ALC feedback loop. The modulator's RF output signal is coupled directly to the Mixer where it is mixed with the LO signal. The difference frequency output is coupled to the 1-1300

Frequency Doubler Section

Doubler Assembly input signal is passed directly to the 10 dB Step Attenuator. At center frequencies greater or equal to 1300 MHz, the frequency. The second harmonic signal is passed through a frequency doubler and tracking bandpass filter, is amplified, and is connected to the 10 dB Step Attenuator.

The difference frequency output from the Mixer Section is coupled to the 1-1300 MHz Amplifier, increased in level by ≈41 dB, and then is coupled to the Frequency Doubler Assembly.

The Frequency Doubler Assembly actually contains the RF Detector circuit. It produces a dc voltage which is proportional to the peak RF output voltage. This signal, which is amplified to drive the front panel meter and the AM Gain compensation circuits in the Reference Assembly, is also coupled to the ALC Amplifier Assembly.

ALC Section

Reference Assembly. In the Local Mode, the RF output level is set by the front panel controls. The unmodulated RF output level follows the ALC loop's dc reference voltage which, in turn, follows the VERNIER control setting.

SERVICE SHEET 2 (Cont'd)

change (modulation characteristics) are dependent on the superimposed modulation drive signal.

In the remote mode, the entire system responds to programmed inputs: the front panel controls of all instruments are inhibited. In the RF Section, the reference output is coupled to the ALC Assembly through the 1 dB Step Attenuator, Therefore, the vernier function is controlled by the 1 dB Step Attenuator.

ALC Amplifier. The ALC Amplifier compares the Detector Amplifier Assembly output to the Reference Assembly output. Any change in the detected RF level or the reference level is immediately reflected at the ALC assembly output. This output is coupled to the A5 Modulator Assembly as the Modulator Bias signal, Because the front panel RF output level is directly proportional to the Modulator RF output level (which is controlled by the series attenuation and consequently the Modulation Bias Signal), the ALC feedback loop is

Pulse Modulation Circuits. During Pulse Modulation, the ALC loop is opened at the ALC Amplifier output. With no signal input, a positive bias voltage to the A5 Modulation Assembly causes the RF signal output to be at least 40 dB down (60 dB down at center frequencies ≥1300 MHz) from the "on-condition". A -10 Vdc pulse biases the RF "on".

Attenuation Section

The Attenuator Section operates identically in local and remote modes. The inputs from the Logic Section (10D, 20D, 40D, and 80D) select the desired attenuation level.

TROUBLESHOOTING

It is assumed that a problem has been isolated to the RF Section as a result of using the System Troubleshooting Guide found in Section VIII of the HP Model 8660-series mainframe Operating and Service Manual and the information entitled System Troubleshooting Service Sheet 1. Troubleshoot the RF Section using the test equipment, information, and procedures which follow.

Test Equipment

Spectrum Analyzer					HP 8555A/8552B/140T
Oscilloscope					HP 180C/1801A/1821A
Digital Voltmeter					HP 3466A

Test 1. It is good practice to first check the power supply inputs to the RF Section and at the same time, it may help to check AM, Pulse ID or any other inputs which relate to the problem. The inputs may be checked at the A12 Assembly test points on the right-side rear of this plug-in. Refer to Figure 8-5.

SERVICE SHEET 2 (Cont'd)

A12 Assembly Test Points

0V 0V 0 V _u	
------------------------------	--

Test 2. If the problem is related to incorrect output level proceed to Test 3. If it is a unique type problem such as amplitude modulation. noise, etc., refer to the following items for additional troubleshoot-

- a. Frequency Problems. In the RF Section, a frequency problem may be caused by a malfunction in the frequency doubling circuitry or its logic control circuitry. If the logic inputs are incorrect, refer to Service Sheet 3; otherwise, refer to Service Sheet 7.
- b. Spurious Signals. May be isolated by checking for signal at various locations in the RF Section, Setting the A4S1 switch to Test may help to isolate the problem to the RF circuitry or ALC loop. Check for oscillations in the A22A2 and A22A3 Assembly amplifiers (refer to Service Sheet 7) and for the Doubler Amplifier Drive Voltage (refer to Service Sheet 12).
- c. Noise. Generally, noise originates in Frequency Extension Module or the A15 20 MHz Amplifier Assembly.
- d. Harmonic Signals. In the RF Section, harmonic signals are usually generated in the Frequency Doubler Assembly, Check the logic inputs. Refer to Service Sheet 3 or 7.
- e. Amplitude Modulation. Verify that the AM signal reaches the A10 Reference Assembly,

If amplitude modulation level changes with an RF level change, check the RF Section front panel meter reading versus measured RF OUTPUT level. If the panel meter reading is correct, refer to Service Sheet 8 (check AM Gain input and related circuits), Otherwise, check the meter driver amplifier and related components shown on Service

Distortion problems may be caused by defective components associated with the ALC Bandwidth Input, Check the logic inputs from Service Sheet 3. Then refer to Service Sheet 3. 6. or 8.

If the amplitude modulation level differs from the level shown, perform the related adjustment procedures in Section V to see if the error is corrected. Be sure the fault isn't in the Modulation Section. An input of 1.0 Vrms to the A10 Reference Assembly should equal

f. Phase Modulation. The output of the A16 Phase Modulator

Service

SERVICE SHEET 2 (Cont'd)

Driver Assembly is a distorted sinusoidal waveform of approximately 7.5 Vp-p for a full scale Modulation Section meter indication. If the output is incorrect, check the output of the cable, W12, to determine if W12 or A16 is defective. The output should be 1.5 Vrms. If the output of the A16 assembly is correct, either W14 or A17 is defective. Refer to the paragraph entitled L.O. Signal Circuits Repair procedure in Section VIII of this manual for disassembly and repair procedures.

Phase modulation distortion problems in the RF section will generally be caused by the A16 Phase Modulator Driver Assembly or the A17 Phase Modulator Assembly, Refer to Service Sheet 5

Excessive incidental AM during phase modulation may be caused by incorrect operation of the 50 MHz Low Pass Filter. Check the control input and the RF output level of the filter. Refer to Service Sheet 4.

- g. Pulse Modulation. Problems may be isolated by checking Pulse In and Pulse ID inputs. Also, check continuity from A5 Modulator Assembly inputs from Auxiliary Section.
- h. Incorrect Front Panel Meter Reading. Refer to Test 3.

Test 3. If the RF output level is incorrect by more than 1 or 2 dB. proceed to Test 4. Otherwise check the 10H input to the A10 Assembly related components, Refer to Service Sheet 3 if the input is incorrect. If necessary, refer to Section V and perform the RF Output Level and 1 dB Step Attenuator Adjustment procedures, If the Adjustments cannot be done or do not correct the tracking across the VERNIER range, check the Meter Driver and Meter circuitry, and the AM Gain circuits. Refer to Service Sheets 6 and 8 respectively. Also check the circuits in the A4 Assembly which are influenced by the 10H input.

Test 4. Proceed to Test 5 if the RF output level is higher than normal. The RF outputs listed in each step of this test (4) are lower than normal. The three voltages shown in parentheses are Modulator Bias Signal ranges. They indicate that the ALC loop (1) is holding the RF output low, (2) is trying to increase the RF output or (3) that a quiescent level, although incorrect, has been reached. Refer to the block diagram for the normal range of Modulator Bias Signal levels.

a. The RF output is low but the ALC loop is trying to increase the level (>-3 Vdc), Check the RF outputs of FL1, A7, A6, and A22 to isolate the problem to Service Sheet 4 (for other than option 002 instruments). Service Sheets 4 or 5 (option 002 instruments only). Service Sheet 6, or Service Sheet 7 respectively.

If the output of FL1 is correct and the output of A7 is incorrect, the

System Troubleshooting Block Diagram ♠ SERVICE SHEET 1

SERVICE SHEET 2 (Cont'd)

problem may be on either Service Sheets 4 or 5 in ... If the output is lower (more positive than normal) option 002 instruments. In this case, refer to the check the 1A, 2A, 4A, and 8A inputs to the A10 LO Signal Circuits Repair procedure and the Assembly (remote mode only). If they are correct Troubleshooting Block Diagram to isolate the or the instrument is in local mode, refer to Service problem to an assembly or cable.

if the output of A7 is defective, refer to Service Service Sheet 3. Otherwise, check the detector Sheet 4.

Each of these assemblies and circuits, if defective, must be replaced as a unit with the exception of A7. If A7 is defective, refer to Service Sheet 4 for test are higher than normal. The voltages enclosed further troubleshooting information.

Vdc). First, check the A10 Reference Assembly and CCW position with A4S1 in the Normal position. If the output is abnormal refer to the

input at A4 pin 11.) Otherwise, Service Sheet 8 Sheet 8 and continue troubleshooting. contains the necessary troubleshooting information.

Modulator Bias Signal

A4S1	Vernier Control Settings												
Switch		С	W		ccw								
	90	14	90)7	904	907							
Normal	+0.2	Vdc	+0.4	Vdc	+1 to +11 Vdc	+0.8 Vde							
Test	-4	Vdc	-3.0	Vdc	+0.3 Vdc	+0.5 Vdc							

Sheet 8. If the remote inputs are incorrect or the On instruments other than option 002 instruments, ator, refer to troubleshooting information on output and reference at A4 pin 10 and 11. Refer to

Model 866034

Test 5. The RF outputs listed in each step of this in parentheses are Modulator Bias Signal ranges. They indicate that the ALC loop (1) is holding the RF output high, (2) is trying to decrease the b. The RF output is low and the ALC loop is holding the Modulator Bias Signal level low (>+10 output level or (3) that a quiescent level, although incorrect, has been reached. Refer to the block output with the VERNIER control set to the CW diagram for normal values of Modulator Bias

- a. High RF output level: the ALC has introubleshooting information on Service Sheet 8. A creased the level (>-3 Vdc). Check the A10 normal output indicates the defect is either on the Reference Assembly output. If the response to A3 ALC Assembly, A22 Frequency Doubler VERNIER control settings is abnormal, refer to Assembly, or the A4 Detector Amplifier Assembly. Service Sheet 8 and troubleshoot the A10 Assembly. If the response is normal, set the A4S1 switch Set the A4S1 switch to the Test position. If the to test. If the Modulator Bias Signal responds to Modulator Bias Signal exhibits the same response the VERNIER control settings as indicated by the as shown in the following table, the problem is table of Test 4b, check that the detector output either in the A22 Frequency Doubler Assembly responds properly to the increased RF signal level which contains the detector or the A4 Detector (check A4 pin 10 and 11) and refer to either Amplifier Assembly, (Check the Detector Signal Service Sheet 6 or 7, Otherwise, turn to Service
 - b. High RF output level; the ALC is trying to decrease the level (>+10 Vdc). The A5 Modulator Assembly or associated circuitry is probably defective (refer to Service Sheet 4).
- c. The Modulator Bias Signal is at a quiescent level but higher (more negative) than normal. Check the A10 Reference Assembly output. If the A10 output is more negative than normal, check the 1A, 2A, 4A, and 8A inputs to the A10 assembly (remote mode only). If the A10 outputs are correct or the instrument is in local mode, refer to Service sheet 8. If the remote inputs are incorrect or the problem is associated with the 10 dB Step Attenuator, refer to the troubleshooting information on Service Sheet 3. Otherwise c. The Modulator Bias Signal is at a quiescent check that the detector output responds properly level but is lower (more positive) than normal. to the increased RF signal level (check A4 pins 10 Check the A10 Reference Assembly output level. and 11). Refer to either Service Sheet 6 or 7.

8-22

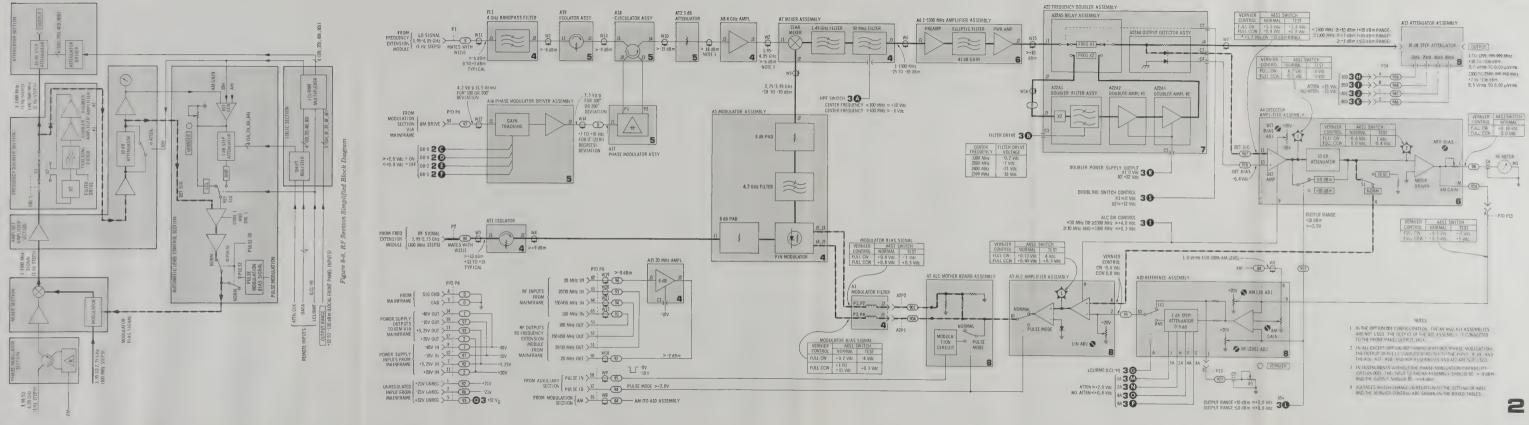


Figure 8-9, Main Troubleshooting Block Diagram

SERVICE SHEET 3 (Cont'd)

Local Mode

In local mode, the inputs mentioned in the preceding paragraph are not used. The 1A, 2A, 4A, and 8A outputs are also not used. (VERNIER control replaces the 1 dB step attenuator.) Check the 1F, 2F, 4F, 8F, and 1H inputs against the levels shown for the S1 switch in the diagram.

Remote Mode

Check the Logic Assembly PI, ATTN CLK, and RESET inputs. Switch to the local mode and then back to the remote mode of operation. Verify that the attenuation level has reset to 150 dB by checking the 10L, 20L, 40L, 80L, and 10H outputs [10H and 10L should be low (<+0.8 Vdc) while 20L, 40L, and 80L should be high (>+2.0 Vdc)]. The momentary low input (0 Vdc as compared to the normal +5 Vdc) may be observed on an oscilloscope at the instant of switching. A logic probe may also be used to verify the presence of the reset pulse. To verify that the PI (data) and

ATTN CLK inputs are correct, program the information shown in the table at the bottom of this page. Check each output for the correct level. If any level is incorrect, the presence of the data and/or the ATTN CLK inputs may be checked at the instant of programming with an oscilloscope or logic probe.

Check the A9 Attenuator Drive Assembly outputs against the inputs.

NOTE

If the problem is isolated between the inputs and outputs of an assembly, refer to the appropriate Service Sheet as indicated on the diagram.

Frequency Doubling Malfunction in the A23 or A24 Assembly (Option 003 Instruments)

Refer to Service Sheet 12 for troubleshooting information.

Programmad	DE Output	Outputs										
Programmed Attenuation	RF Output Level	1A 1 dB	2A 2 dB	4A 4 dB	8A 8 dB	10L 10 dB	20L 20 dB	40L 40 dB	80L 80 dB	10H 10 dB		
7 dB	+6 dBm	Н	Н	Н	L	L	L	L	L	L		
87 dB	-74 dBm	Н	Н	Н	L	Н	Н	Н	L	Н		
98 dB	-85 dBm	L	L	L	Н	L	L	L	Н	Н		

H = Attenuation = >+2.0 Vdc

L = No Attenuation = <+0.8 Vdc

NOTE

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting Guide). Then, if that information indicates possible problems in the RF Section, refer to the Systems Troubleshooting information (Service Sheet 1). This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe. If the problem is in this plug-in, refer to Service Sheet 2 for further troubleshooting information.

MIXER SECTION

PRINCIPLES OF OPERATION

General

The LO signal is filtered and amplified to drive the mixer. The RF signal is leveled and may be amplitude modulated at the A5 Modulator Assembly. After passing through the Modulator, the RF Signal and LO Signal are mixed; the difference frequency is passed on for further amplification.

4 GHz Bandpass Filter/Amplifier

Unwanted sidebands are eliminated from the LO signal by passing the signal through a bandpass filter. In option 002 instruments, the LO signal is coupled to the phase modulation circuits before being input to the 4 GHz Amplifier. The signal is amplified to a high level to drive the mixer.

Isolator

The 3.95 to 2.75 GHz RF Signal is passed through the Isolator to the Modulator Assembly. Reverse signal attenuation is about 20 dB.

Modulator Assembly

The effect of the PIN Diode Modulator on the RF Signal is that of a variable attenuator. The level of attenuation and therefore the modulator RF output is dependent on the Modulator Bias Signal dc level.

The PIN Diode Modulator has dynamic attenuation range of >50 dB. A more positive modulator bias signal turns off the series diodes while the shunt diodes are forward biased. The shunt diodes and the series resistor form a voltage divider which attenuates the RF Signal. As the bias voltage goes more negative, the impedance of the shunt diodes increases while the series diodes impedance decreases. Therefore, the RF signal attenuation decreases. The shunt diodes effectively control the attenuation from 12 to >50 dB down while the series diodes are effective only to about 12 dB down.

NOTE

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting Guide). Then, if that information indicates possible problems in the RF Section, refer to the System Troubleshooting information in Service Sheet 1. This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe, If the problem is in this plug-in, return to Service Sheet 2 for further troubleshooting information.

LOGIC CIRCUITRY

PRINCIPLES OF OPERATION

General

In this instrument, the logic inputs to the analog circuits control functions such as frequency doubling and attenuation of the RF output signal. These inputs also influence the phase modulation and ALC bandwidth.

In the remote mode, all control signals are external to the RF Section. In the local mode, the OUTPUT RANGE switch selects the range by using a binary coded hexadecimal output with an extra overrange line. Also, the VERNIER control is analog in nature in the

Filter Driver Assembly

The eighth, ninth, and tenth digit BCD inputs from the mainframe (10 MHz, 100 MHz, and 1 GHz) are used in the frequency doubling mode. These inputs are applied to digital-to-analog converters. The converter's outputs are input to summing amplifiers to produce an analog output which drives a tracking bandpass filter. The filter separates the second harmonic of the RF signal from its fundamental and other harmonics to produce the desired output frequency.

A decoder circuit determines when the frequency output from the A7 Assembly is greater than 100 MHz, The A7A5 50 MHz High Pass Filter is switched on effectively trapping any low frequency phase modulation drive signals which would otherwise be amplified and passed on to the RF output.

Logic Assembly

Local operation of the 10 dB Step Attenuator is selected by a logic high on the LCL/RMT input. Thus, control of the 10 dB Step Attenuator by the inputs from the front panel OUTPUT RANGE switch is enabled while the remote inputs are inhibited,

In Remote mode, a logic low in the LCL/RMT inputs inhibits front panel control and enables data information flow from the mainframe

SERVICE SHEET 3 (Cont'd)

to the Logic Assembly. The ATTN CLK controls the data inputs on the PI-1, PI-2, PI-4, and PI-8 lines to the Logic Assembly. The OUTPUTS to the 10 dB Step Attenuator (10L, 20L, 40L, 80L), the over-range (10H), and the 1 dB Step Attenuator outputs (1A, 2A, 4A. 8A) are all controlled by external programming in the Remote Mode. A safety feature, the RESET input, sets the 10 dB Step Attenuator to the maximum attenuation when the Remote mode of operation is first initiated.

Attenuator Driver Assembly

The inputs from the Logic Assembly (101, 201, 401, and 801) switch the equivalent attenuator drive outputs (10D, 20D, 40D, and 80D). These outputs provide the higher voltages and current needed to drive the relays in the Attenuator Assembly.

Doubler Power Supply Assembly

This assembly provides three outputs which are selected by two inputs from the mainframe. The inputs are set by the system center frequency, At ≥1300 MHz (X2 range), the Doubler Power Supply output connects the +22 Vdc to two RF amplifiers in the Frequency Doubler Assembly, Also, at or above 1300 MHz, +12 Vdc is connected to a relay in the Frequency Doubler Assembly. The Bandwidth Control is switched at center frequencies of 10 MHz or 1300 MHz.

Ontion 003 Instruments

In option 003 instruments, the A23 Doubler Logic and A24 Frequency Doubler Test Switch Assemblies are added. These circuits allow front panel selection of the frequency range (X1 and X2) when the RF Section is used with 8660A or 8660B mainframes.

TROUBLESHOOTING

Malfunctions in the RF Section which appear to be a logic problem may be an analog circuit problem. Refer to Service Sheet 2 to begin troubleshooting.

Test Equipment

Digital Voltmeter. HP 3466A Logic Probe HP 10525T

General

If the malfunction is isolated to the logic circuits, the related inputs must be checked before an attempt is made to troubleshoot the individual circuit assemblies. The control levels are fixed and may change when a new center frequency or mode of operation (local or remote) has been selected. The clocked or momentary inputs, PI (plug-in), ATTN CLK, and RESET occur only at the instant the center frequency or mode change is made.

> Main Troubleshooting Block Diagram SERVICE SHEET 2

SERVICE SHEET 3 (Cont'd)

Local Mode

In local mode, the inputs mentioned in the preceding paragraph are not used. The 1A, 2A, 4A. and 8A outputs are also not used, (VERNIER control replaces the 1 dB step attenuator.) Check the 1F, 2F, 4F, 8F, and 1H inputs against the levels shown for the S1 switch in the diagram.

Remote Mode

Check the Logic Assembly PI, ATTN CLK, and RESET inputs, Switch to the local mode and then back to the remote mode of operation. Verify that the attenuation level has reset to 150 dB by checking the 10L, 20L, 40L, 80L, and 10H outputs [10H and 10L should be low (<+0.8 Vdc) while 20L, 40L, and 80L should be high (>+2.0 Vdc)]. The momentary low input (0 Vdc as compared to the normal +5 Vdc) may be observed on an oscilloscope at the instant of switching. A logic probe may also be used to verify the presence Refer to Service Sheet 12 for troubleshooting of the reset pulse. To verify that the PI (data) and information.

ATTN CLK inputs are correct, program the information shown in the table at the bottom of this page. Check each output for the correct level. If any level is incorrect, the presence of the data and/or the ATTN CLK inputs may be checked at the instant of programming with an oscilloscope or

Check the A9 Attenuator Drive Assembly outputs against the inputs.

NOTE

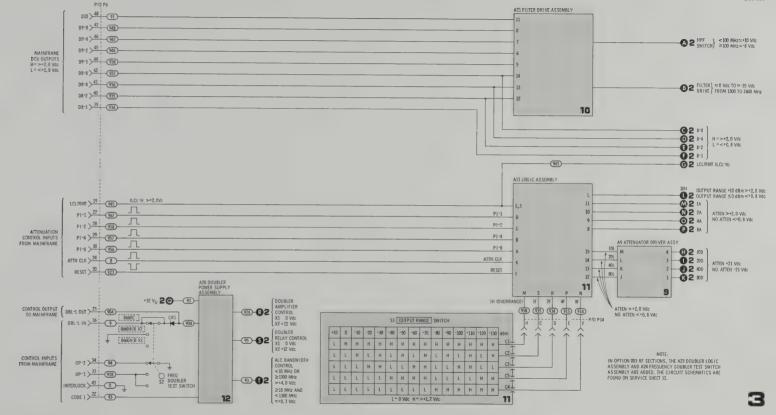
If the problem is isolated between the to the appropriate Service Sheet as indicated on the diagram.

Frequency Doubling Malfunction in the A23 or A24 Assembly (Option 003 Instruments)

	DE O	Outputs												
ogrammed tenuation	RF Output Level	1A 1 dB	2A 2 dB	4A 4 dB	8A 8 dB	10L 10 dB	20L 20 dB	40L 40 dB	80 dB	10H 10 dB				
7 dB	+6 dBm	Н	Н	Н	L	L	L	L	L	Ĺ				
87 dB	-74 dBm	Н	Н	Н	L	Н	н	Н	L	Н				
98 dB	-85 dBm	L	L	L	Н	L	L	L	Н	Н				

H = Attenuation = >+2.0 Vdc

L = No Attenuation = <+0.8 Vdc



SERVICE SHEET 4 (Cont'd)

The RF output level at the front panel jack is directly proportional to the Modulator Assembly RF output. The Modulator Bias Signal controls the A5 Modulator Assembly output and is dependent on an error voltage derived from comparing the RF detector output to the reference dc level.

Mixer Assembly

The RF Signal is passed through a low pass filter and attenuator before leaving the Modulator Assembly. Then the RF signal is mixed with the LO signal in the Mixer Assembly, the mixer output passes through a low pass filter, and the difference frequency is a 1-1300 MHz phase-locked signal with frequency resolution of 1 Hz.

At center frequencies ≥ 100 MHz, the High Pass Filter Control input to the A7A5 Assembly causes the mixer output to pass through the 50 MHz High Pass Filter. This reduces incidental AM distortion generated by the phase modulated signal in the balanced mixer.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2 was used to isolate a circuit defect to the assemblies or cables shown on the accompanying diagram. Troubleshoot the Mixer Section by using the test equipment and procedures given below.

NOTE

In Option 002 instruments, a defect cannot easily be isolated to circuits

shown on this schematic diagram, Refer to Service Sheet 2 and the repair procedure entitled LO Signal Circuits Repair,

Test Equipment

Spectrum Analyzer . . HP 8555A/8552B/140T

Power Meter. HP 435A/8481A

Digital Voltmeter . . . HP 3466A Service Kit HP 11672A

Test 1. Check the power supply inputs to the A8 Assembly (+20V and -10V). If correct, proceed to Test 2. Otherwise check for continuity of interconnections to mainframe or an A8 Assembly defect.

CAUTION

Slight but repeated bending of semi-rigid coaxial cables will damage them very quickly. Bend the cables as little as possible. If necessary, loosen the assembly to release the cable.

Test 2. If the RF power output is greater than normal (refer to the schematic), the A5 Modulator Assembly is probably defective. If the power output is less than normal, checking the difference assembly outputs will quickly isolate the defective assembly or cable.

NOTE

Defects in the A15 20 MHz Amplifier Assembly and RF interconnections from mainframe to Frequency Extension Module (through the RF Section) normally will be isolated by using the Systems Troubleshooting (Service Sheet 1).

A7A1-

SERVICE SHEET 5 (Cont'd)

A17 Phase Modulator Assembly

In the phase modulator, the LO signal passes through the blocking capacitors and down the stripline transmission lines to the varactor diode terminations, A17CR1 and CR2. The amount of phase shift between the incident and reflected signals is determined by the varactor capacitance.

The varactor capacitance is voltage variable. The dc bias input sets the quiescent phase shift. The instantaneous phase shift is dependent on the sum of the dc bias and the ac modulation drive signal input to the phase modulator.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2 and the LO Signal Circuits Repair procedure were used to isolate the defect to one of the Assemblies. Troubleshoot the A16 or A17 Assemblies by using the following procedure.

Test Equipment

A16 and A17 Assembly circuit malfunctions usually result in incorrect or no modulation drive, incorrect gain tracking, or unwanted distortion. Distortion may be due to misadjusted or defective components.

Set the system's modulation section switches for ϕM mode, internal 1 kHz source, and adjust the modulation level control for a full scale meter reading (100° or 200°). Refer to the schematics for the typical voltages.

A2 ALC Mother Board Assembly
A5 Modulator Assembly
A7 Mixer Assembly
A8 4 GHz Amplifier Assembly
A12 Logic Mother Board Assembly
A15 20 MHz Amplifier Assembly
AT1 Isolator
FL1 4 GHz Band Pass Filter

SERVICE SHEET 4

A1 Modulator Filter Assembly

NOTE

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting Guide). Then, if that information indicates possible problems in the RF Section, refer to the Systems Troubleshooting information (Service Sheet 1), This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe, If the problem is in this plug-in, refer to Service Sheet 2 for further troubleshooting information

MIXER SECTION

PRINCIPLES OF OPERATION

General

The LO signal is filtered and amplified to drive the mixer. The RF signal is leveled and may be amplitude modulated at the A5 Modulator Assembly, After passing through the Modulator, the RF Signal and LO Signal are mixed; the difference frequency is passed on for further amplification.

4 GHz Bandpass Filter/Amplifier

Unwanted sidebands are eliminated from the LO signal by passing the signal through a bandpass filter. In option 002 instruments, the LO signal is coupled to the phase modulation circuits before being input to the 4 GHz Amplifier. The signal is amplified to a high level to drive the mixer.

Isolator

The 3.95 to 2.75 GHz RF Signal is passed through the Isolator to the Modulator Assembly, Reverse signal attenuation is about 20 dB.

Modulator Assembly

The effect of the PIN Diode Modulator on the RF Signal is that of a variable attenuator. The level of attenuation and therefore the modulator RF output is dependent on the Modulator Bias Signal dc

The PIN Diode Modulator has dynamic attenuation range of >50 dB. A more positive modulator bias signal turns off the series diodes while the shunt diodes are forward biased. The shunt diodes and the series resistor form a voltage divider which attenuates the RF Signal. As the bias voltage goes more negative, the impedance of the shunt diodes increases while the series diodes impedance decreases. Therefore, the RF signal attenuation decreases. The shunt diodes effectively control the attenuation from 12 to >50 dB down while the series diodes are effective only to about 12 dB down.

SERVICE SHEET 4 (Cont'd)

Service

The RF output level at the front panel jack is directly proportional to the Modulator Assembly RF output. The Modulator Bias Signal controls the A5 Modulator Assembly output and is dependent on an error voltage derived from comparing the RF Test Equipment detector output to the reference dc level.

Mixer Assembly

The RF Signal is passed through a low pass filter and attenuator before leaving the Modulator Assembly. Then the RF signal is mixed with the LO signal in the Mixer Assembly, the mixer output passes through a low pass filter, and the difference frequency is a 1-1300 MHz phase-locked signal with frequency resolution of 1 Hz.

At center frequencies ≥100 MHz, the High Pass Filter Control input to the A7A5 Assembly causes the mixer output to pass through the 50 MHz High Pass Filter. This reduces incidental AM distortion generated by the phase modulated signal in the balanced mixer.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2 was used to isolate a circuit defect to the assemblies or cables shown on the accompanying diagram, Troubleshoot the Mixer Section by using the test equipment and procedures given below.

NOTE

In Option 002 instruments, a defect cannot easily be isolated to circuits

shown on this schematic diagram. Refer to Service Sheet 2 and the repair procedure entitled LO Signal Circuits Repair.

Spectrum Analyzer . . HP 8555A/8552B/140T Power Meter, . . . HP 435A/8481A Digital Voltmeter . . HP 3466A Service Kit HP 11672A

Test 1. Check the power supply inputs to the A8 Test 2. Otherwise check for continuity of interconnections to mainframe or an A8 Assembly defect.

Slight but repeated bending of semi-rigid coaxial cables will damage them very quickly. Bend the cables as little as possible. If necessary, loosen the assembly to release the cable.

Test 2. If the RF power output is greater than normal (refer to the schematic), the A5 Modulator Assembly is probably defective. If the power output is less than normal, checking the difference assembly outputs will quickly isolate the defective assembly or cable.

NOTE

Defects in the A15 20 MHz Amplifier Assembly and RF interconnections from mainframe to Frequency Extension Module (through the RF Section) normally will be isolated by using the Systems Troubleshooting (Service Sheet 1).

A7A1

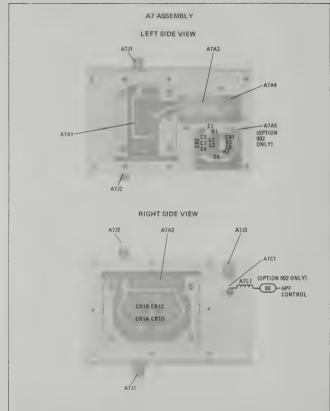
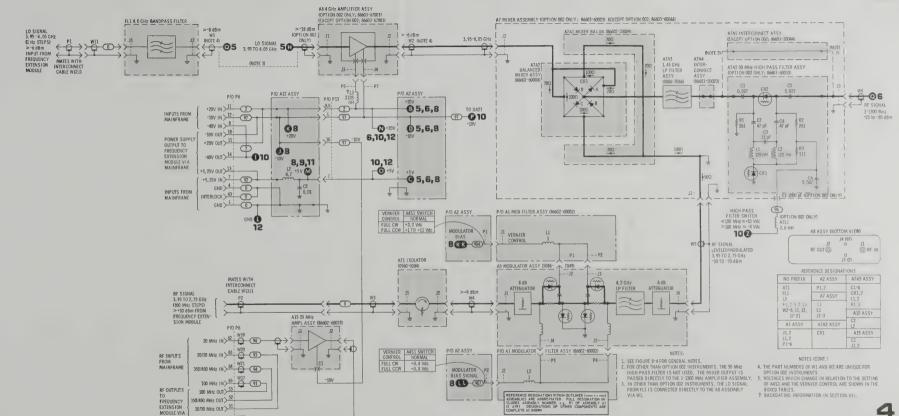


Figure 8-11. A7 Mixer Assembly's Subassembly and Component Locations



MAINFRAME

Figure 8-12. Mixer Section Schematic Diagram

A1, A2, A5, A7, A8, A12, A15, AT1, FL1

SERVICE SHEET 5 (Cont'd)

A16 Assembly

- **Test 1.** Check the power supply inputs to the A16 Assembly.
- **Test 2.** Check the peak-to-peak ac voltages at the various points as indicated on the schematic. If all seem to be correct, refer to Section V and readjust the phase modulation circuits.
- **Test 3.** If the output of the discrete component operational amplifier is defective, check the dc output and compare it to the dc inputs. If the change in dc output voltage from normal does not follow the change in input dc voltage, the problem is probably in Q4 thru Q10 or their associated

- components. For example, the output voltage is more positive than normal.
- **Test 4.** Check the dc voltages on A16Q1 through Q3 and Q11.
- **Test 5.** If the gain tracking is incorrect, check and compare the inputs and outputs of A16U1 and U2.

A17 Assembly

- **Test 1.** Remove the assembly cover. Check for the presence of the dc bias and ac voltage on the varactor diodes, A17CR1 and CR2.
- **Test 2.** Verify that A17C1 and C3 are not defective.

NOTE

When a malfunction occurs, refer to Section VIII of the Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (Systems Troubleshooting Guide). Then, if that information indicates possible problems in the RF Section, refer to the Systems troubleshooting information in Service Sheet 1 in this manual. This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe. If the problem is in this plug-in, refer to Service Sheet 2 for further troubleshooting information.

PRINCIPLES OF OPERATION

1 - 1300 MHz Amplifier Assembly

The A6 1-1300 MHz Amplifier Assembly contains an RF Preamplifier and Amplifier which are separated by an elliptic low pass filter. The combined RF gain is approximately 41 dB.

Detector Amplifier Assembly

A small bias current through the RF Detector and Reference Diodes in the A22 Assembly is set by the A4R13 Detector Bias Adjustment for maximum detector sensitivity. Beyond the initial bias current, any further change in current flow is due to temperature variations. Because the two diodes are located in the same thermal environment, an increase in current flow through the RF Detector Diode is matched by an equal increase in current flow through the Reference Diode. The Reference Diode current is coupled to the non-inverting input of the Detector Amplifier (a discrete operational amplifier comprised of A4Q3, A4Q2, A4Q1 and associated components) while the RF Detector Diode output is coupled to the inverting input. Therefore, any change in current flow due to a change in temperature is cancelled in the operational amplifier which leaves the output level dependent only on the peak RF output from the A22 Assembly.

At center frequencies of <10 MHz and >1300 MHz, the ALC Bandwidth Control input causes A4Q4 to be biased on which connects A4C3 in parallel with the 47 pF capacitor found in the A22A4 Assembly. As the center frequency is decreased, the detector output needs to be retained for a longer period of time so the leveling circuit responds to the average RF level rather than the instantaneous level. In the doubled frequency mode (>1300 MHz), the ALC bandwidth must be reduced to insure ALC loop stability.

In output ranges of \leq 0 dBm, the Detector Amplifier is coupled directly to the A3 ALC Amplifier Assembly. The output is compared

A16 Phase Modulator Driver Assembly
A17 Phase Modulator Assembly
A18 Circulator Assembly
A19 3.9-4.1 GHz Isolator Assembly
AT2 3 dB Attenuator
SERVICE SHEET 5 (Option 002)

Figure 8-1

mum gain).

SERVICE SHEET 5 (Cont'd)

duced to compensate for the phase modulator's inability to produce a constant phase deviation at different LO frequencies. At higher LO frequencies, the phase modulator sensitivity is lower and a higher level modulation drive signal is required to produce the same phase deviation. The modulation drive signal level is changed, with respect to the LO frequency, by the digitally controlled attenuator A16U1 and differential amplifiers A16Q1 and Q2. At system center frequencies where digit 8 (10 MHz steps) is zero (LO frequency is 3.95 MHz) logic lows (< +0.8 Vdc) are present at inputs to A16U1. Lows cause cause the attenuator stage to be off with minimum attenuation of the signal at the junction of A16R12, R13. The differential voltage across the bases of A16Q1 is essentially zero and the gain is unity. When an input to A16U1 is high the transistor stage is turned on. current flows from the modulator drive signal path through either A16R4, R6, R8, or R10. Any difference in amplitude between the bases of A16Q1 is amplified and coupled to A16Q2 where it is further amplified. The differential output voltage across A16R27 is coupled to the gate of A16Q4. The gain control, A16R2, sets the modulation level at 3.95 GHz (unity gain). The Gain Tracking control adjusts the rate of change of attenuation with respect to the LO

J-FET Shaping Circuit. The J-FET A16Q4 is biased so it introduces second order distortion to the modulation drive signal. This distortion compensates for the second order distortion in the transfer characteristics of the phase modulator. The transfer characteristics of the phase modulator are varied by changing the dc output from the A16 Assembly. The Second Harmonic Adjust Control A16R36 sets the second order distortion level of A16Q4 (by controlling the drain current flow) and the dc output from A16 (which is proportional to the A16Q4 drain voltage). The distortion level is set by demodulating the system's RF output and nulling the second order harmonic distortion.

frequency by setting the phase modulation level at 4.05 GHz (maxi-

Modulation Driver Amplifier. The J-FET output is coupled to the discrete component operational amplifier made up of A16O5 through Q7 and their associated components. The amplifier's high frequency rolloff is set by A16C7. The gain of approximately 10 is determined primarily by A16R49, 1000Q, and A16R38, 110Q The network of A16RT1, A16R38 and R39 aid in reducing gain changes due to J-FET drift with temperature.

Service

SERVICE SHEET 5 (Cont'd)

A16 Assembly

Test 1. Check the power supply inputs to the A16 Assembly.

Test 2. Check the peak-to-peak ac voltages at the various points as indicated on the schematic. If all seem to be correct, refer to Section V and readjust the phase modulation circuits.

Test 3. If the output of the discrete component Test 1. Remove the assembly cover. Check for the operational amplifier is defective, check the dc presence of the dc bias and ac voltage on the output and compare it to the dc inputs. If the varactor diodes, A17CR1 and CR2. change in dc output voltage from normal does not follow the change in input dc voltage, the problem Test 2. Verify that A17C1 and C3 are not deis probably in Q4 thru Q10 or their associated fective.

components. For example, the output voltage is more positive than normal.

Test 4. Check the dc voltages on A16Q1 through Q3 and Q11.

Model 866034

Test 5. If the gain tracking is incorrect, check and

A17 Assembly

NOTE

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting lems in the RF Section, refer to the Systems Troubleshooting information which precedes Service Sheet 1. This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe. If the problem is in this plug-in, refer to Service Sheet 1 for further troubleshooting information.

PRINCIPLES OF OPERATION

General

The phase modulation drive signal from the modulation section is coupled to the A16 Phase Modulation Driver Assembly. The signal is predistorted and the overall gain is varied (with respect to LO frequency) to compensate for the frequency sensitivity of the A17 Phase Modulator Assembly. The signal is amplified before being connected to the phase modulator.

With minimal loss, the LO signal passes through the A19 3.9-4.1 GHz Isolator Assembly to the A18 Circulator Assembly. The signal passes from port 1 to port 2 and on to the phase modulator.

In the phase modulator, the varactor diode, A17CR1, reactively terminates the stripline transmission line which reflects the LO signal. Changing the bias voltage applied to the varactor diode changes the termination reactance. This cuases the reflected signal to shift in phase with respect to the incident input signal.

The reflected LO signal travels back down the transmission line and through port 2 to port 3, where it again enters the phase modulator. The same sequence of events occurs. Thus, the phase shift of the LO signal reflected back to port 3 is approximately doubled.

The phase modulated LO signal continues from port 3 to port 4, through the AT2 3 dB Attenuator and on to the A8 4 GHz Amplifier Assembly, Due to the high input reflection coefficient of the 4 GHz Amplifier, a large portion of the signal is reflected back to port 4, through to port 1, and on to the Frequency Extension Module. The AT2 3 dB Attenuator and A19 3.9-4.1 GHz Isolator Assemblies reduce the level of the reflected signal to minimize the interference created in the extension module VCO circuits.

A16 Phase Modulator Driver Assembly

The shunt capacity of W12 and A16L1 forms a low pass filter which improves the frequency response of the input modulation drive signal up to 10 MHz.

SERVICE SHEET 5 (Cont'd)

A17 Phase Modulator Assembly

In the phase modulator, the LO signal passes through the blocking capacitors and down the stripline transmission lines to the varactor diode terminations, A17CR1 and CR2. The amount of phase shift between the incident and reflected signals is determined by the varactor capacitance.

The varactor capacitance is voltage variable. The dc hias input sets the quiescent phase shift. The instantaneous phase shift is dependent on the sum of the dc bias and the ac modulation drive signal input to the phase modulator.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2 and the LO Signal Circuits Repair procedure were used to isolate the defect to one of the Assemblies, Troubleshoot the A16 or A17 Assemblies by using the following procedure.

Test Equipment

Digital Voltmeter.					HP 3466A
Oscilloscope					HP 180C/1801A/1821A
Spectrum Analyzer					HP 8555 A /8559 R /1 40T

A16 and A17 Assembly circuit malfunctions usually result in incorrect or no modulation drive, incorrect gain tracking, or unwanted distortion. Distortion may be due to misadjusted or defective components.

Set the system's modulation section switches for \$\phi M\$ mode, internal 1 kHz source, and adjust the modulation level control for a full scale meter reading (100° or 200°). Refer to the schematics for the typical

> A1 Modulator Filter Assembly A2 ALC Mother Board Assembly A5 Modulator Assembly A7 Mixer Assembly A8 4 GHz Amplifier Assembly A12 Logic Mother Board Assembly A15 20 MHz Amplifier Assembly AT1 Isolator FL1 4 GHz Band Pass Filter SERVICE SHEET 4

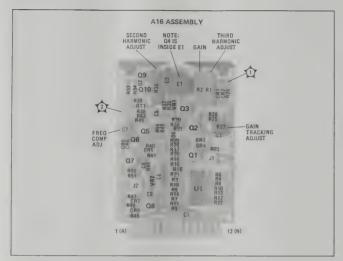


Figure 8-13. A16 Phase Modulator Driver Assembly Component and Test Point Locations

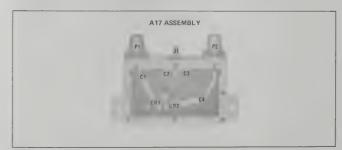


Figure 8-14, A17 Phase Modulator Assembly Component Locations

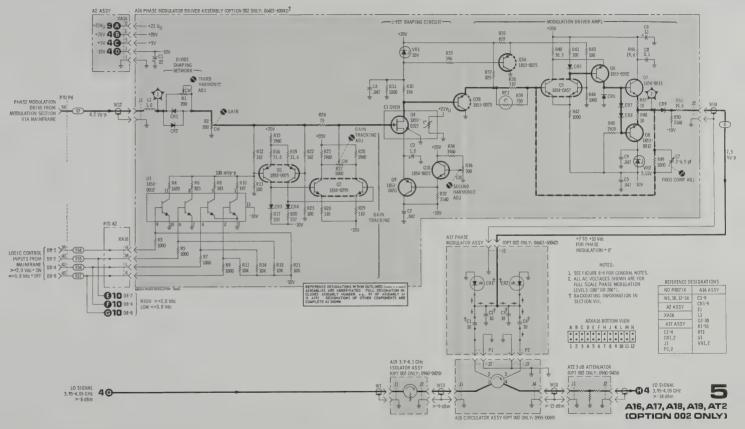


Figure 8-15, Phase Modulation Section Schematic Diagram (Option 002)

Service Model 86603A

SERVICE SHEET 6 (Cont'd)

to a dc reference level and an error signal results which is coupled to the A5 Modulator Assembly to complete the ALC loop. When OUTPUT RANGE switch is set to +10 dBm, the 10H logic input goes high ($\approx+5$ Vdc) and turns A4Q5 off. Relay A4K1 opens and the dc voltage is attenuated 10 dB by A4R19, A4R20, A4R21, and resistors on the A3 assembly. The RF output signal increases 10 dB which brings the dc output to the A3 ALC Amplifier input back to the quiescent level present before switching to the +10 dBm range.

Amplifier A4U1 functions as an active low pass filter because of A4R23 and A4C5 which are connected in the feedback loop. The amplifier drives the meter and provides a compensating dc level which varies the AM drive input to keep the amplifier modulation level constant with change in RF output level (VERNIER Control setting).

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2 was used to isolate a circuit defect to the assemblies shown on the accompanying diagram. Troubleshoot the Detector Amplifier Assembly by using the test equipment and procedures given below.

Test Equipment

Spectrum Analyzer . . HP 8555A/8552B/140T Digital Voltmeter . . . HP 3466A

Test 1. If the circuit problem is associated with the meter and AM Gain output rather than the RF Output level, proceed to Test 2. Check the Detector Output, Detector Amplifier Output A4TP1, and output to ALC Amplifier to see if they are tracking the RF output level. Set A4S1 to the test position. If the RF Amplifier output remains low, the A6 assembly or an associated cable is probably defective. If the RF output increases, measure the detector and A4TP1 and A4TP2 voltages. If the detector output doesn't respond properly, the A22 assembly or an associated input component on the A4 assembly, is probably defective. If the detector output increases but the A4TP1 voltage doesn't go more negative, the detector amplifier or an associated component is probably defective.

If the RF output level is incorrect only in the +10 dBm range or is correct only in the +10 dBm range, and the 10H input is correct for all ranges, the 10 dB attenuator, the relay (A4K1), or an associated component is probably defective.

Test 2. Monitor the RF output with a Spectrum Analyzer. If the modulation level changes with respect to the RF carrier amplitude (change the VERNIER control to three or four different settings), A4U1 or associated components are probably defective. Otherwise, the meter control is misadjusted or the meter connections or an associated component is probably defective.

NOTE

When a malfunction occurs, refer to Section VIII of the Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (Systems Troubleshooting Guide). Then, if that information indicates possible problems in the RF section, refer to the Systems troubleshooting information on Service Sheet 1 in this manual. This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe. If the problem is in this plug-in refer to Service Sheet 2 for further troubleshooting information.

PRINCIPLES OF OPERATION (A22 FREQUENCY DOUBLER ASSEMBLY)

The input RF signal to the frequency doubler is connected directly to the A22A5 Relay Assembly. In the X1 mode, the 1-1300 MHz signal is switched to the A22A4 Output Detector Assembly and on through A22A4R3 and C2 to the 10 dB Step Attenuator Assembly.

In the X2 mode, a logic high (+12 Vdc) appears on the Doubler Relay Control input. This causes the relay A22A5K1 to switch the input signal (650 to <1300 MHz) to the A22A1 Doubler/Filter Assembly. The signal passes through a balun to the bridge rectifier Frequency Doubler, A22A1CR1. The balanced doubler suppresses the fundamental input and odd harmonics while generating a large second harmonic component. A22A1L1 provides a ground return for the dc component of the output signal and R1, R2, and R3 provide RF termination. The output signal passes to the tracking filter. The lead inductance and voltage variable capacitance of the varactor form a series resonant circuit. The Filter Drive input causes the resonant frequency to track the doubled input frequency. The fundamental, odd harmonics, and even harmonics (\geq 4th) are further attenuated but the second harmonic, (\geq 1300 to <2600 MHz) is passed on to the A22A2 Doubler Amplifier Assembly.

In both the A22A2 and A22A3 amplifiers, the doubled RF signal is amplified by at least 10 dB. The A22A3 output is coupled back through the A22A5 and A22A4 Assemblies and on to the 10 dB Step Attenuator.

The RF signal level is detected and a relative dc level proportional to the RF level is coupled to the inverting differential amplifier in the A4 Detector Amplifier Assembly. The reference diode, which is in the same thermal environment as the detector diode, provides temperature compensation for the detector diode because it is coupled to the non-inverting input of the differential amplifier.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2

NOTE

When a malfunction occurs, refer to Section VIII of the Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (Systems Troubleshooting Guide). Then, if that information indicates possible prob-Jems in the RF Section, refer to the Systems troubleshooting information in Service Sheet 1 in this manual. This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe, If the problem is in this plug-in refer to Service Sheet 2 for further troubleshooting information.

PRINCIPLES OF OPERATION

1 - 1300 MHz Amplifier Assembly

The A6 1-1300 MHz Amplifier Assembly contains an RF Preamplifier and Amplifier which are separated by an elliptic low pass filter. The combined RF gain is approximately 41 dB.

Detector Amplifier Assembly

A small bias current through the RF Detector and Reference Diodes in the A22 Assembly is set by the A4R13 Detector Bias Adjustment for maximum detector sensitivity. Beyond the initial bias current, any further change in current flow is due to temperature variations. Because the two diodes are located in the same thermal environment, an increase in current flow through the RF Detector Diode is matched by an equal increase in current flow through the Reference Diode. The Reference Diode current is coupled to the non-inverting input of the Detector Amplifier (a discrete operational amplifier comprised of A4Q3, A4Q2, A4Q1 and associated components) while the RF Detector Diode output is coupled to the inverting input. Therefore, any change in current flow due to a change in temperature is cancelled in the operational amplifier which leaves the output level dependent only on the peak RF output from the A22 Assembly.

At center frequencies of <10 MHz and ≥1300 MHz, the ALC Bandwidth Control input causes A4Q4 to be biased on which connects A4C3 in parallel with the 47 pF capacitor found in the A22A4 Assembly. As the center frequency is decreased, the detector output needs to be retained for a longer period of time so the leveling circuit responds to the average RF level rather than the instantaneous level. In the doubled frequency mode (>1300 MHz), the ALC bandwidth must be reduced to insure ALC loop stability.

In output ranges of ≤0 dBm, the Detector Amplifier is coupled directly to the A3 ALC Amplifier Assembly. The output is compared

> A16 Phase Modulator Driver Assembly A17 Phase Modulator Assembly A18 Circulator Assembly A19 3.9-4,1 GHz Isolator Assembly AT2 3 dB Attenuator SERVICE SHEET 5 (Option 002)

SERVICE SHEET 6 (Cont'd)

Service

to a dc reference level and an error signal results Test 1. If the circuit problem is associated with which brings the dc output to the A3 ALC before switching to the +10 dBm range.

Amplifier A4U1 functions as an active low pass ated input component on the A4 assembly, is filter because of A4R23 and A4C5 which are probably defective. If the detector output increases connected in the feedback loop. The amplifier but the A4TP1 voltage doesn't go more negative, drives the meter and provides a compensating dc the detector amplifier or an associated component level which varies the AM drive input to keep the is probably defective. amplifier modulation level constant with change in RF output level (VERNIER Control setting).

TROUBLESHOOTING

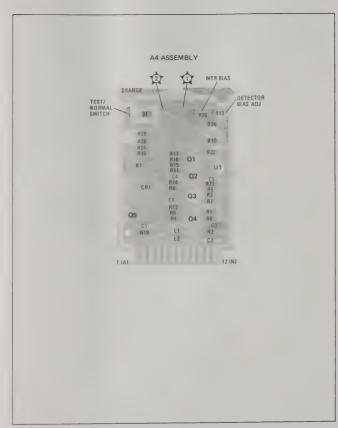
It is assumed that the troubleshooting information on Service Sheet 2 was used to isolate a circuit defect to the assemblies shown on the accompanying diagram. Troubleshoot the Detector Amplifier Assembly by using the test equipment and procedures given below.

Spectrum Analyzer . . HP 8555A/8552B/140T Digital Voltmeter . . . HP 3466A

which is coupled to the A5 Modulator Assembly to the meter and AM Gam output rather than the RF complete the ALC loop. When OUTPUT RANGE Output level, proceed to Test 2. Check the switch is set to +10 dBm, the 10H logic input goes Detector Output, Detector Amplifier Output high (≈+5 Vdc) and turns A4Q5 off. Relay A4K1 A4TP1, and output to ALC Amplifier to see if opens and the dc voltage is attenuated 10 dB by they are tracking the RF output level. Set A4S1 to A4R19, A4R20, A4R21, and resistors on the A3 the test position. If the RF Amplifier output assembly. The RF output signal increases 10 dB remains low, the A6 assembly or an associated cable is probably defective. If the RF output Amplifier input back to the quiescent level present increases, measure the detector and A4TP1 and A4TP2 voltages. If the detector output doesn't respond properly, the A22 assembly or an associ-

> dBm range or is correct only in the +10 dBm range. and the 10H input is correct for all ranges, the 10 dB attenuator, the relay (A4K1), or an associated

Test 2. Monitor the RF output with a Spectrum Analyzer, If the modulation level changes with respect to the RF carrier amplitude (change the VERNIER control to three or four different settings). A4U1 or associated components are probably defective. Otherwise, the meter control is misadjusted or the meter connections or an associated component is probably defective.



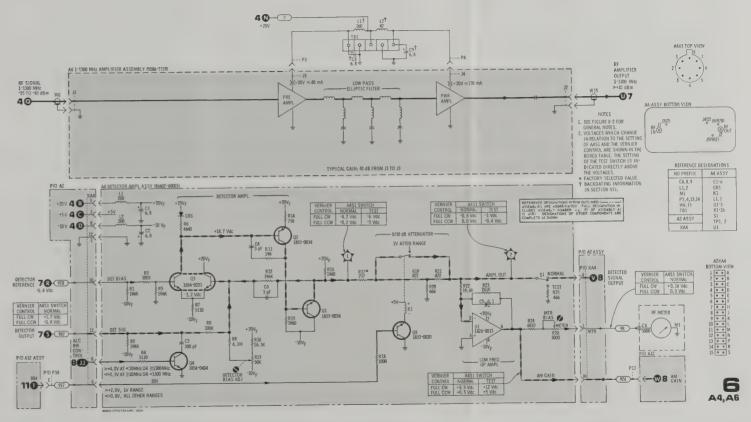


Figure 8-17. 1-1300 MHz Amplifier/Detector Amplifier Schematic Diagram

SERVICE SHEET 7 (Cont'd)

was used to isolate a circuit defect to the assemblies and cables shown on the schematic diagrams. Troubleshoot the frequency doubler circuits by using the test equipment and procedures given below.

Test Equipment

Spectrum Analyzer . . HP 8555A/8552B/140T

BNC Connector . . . HP 1250-0118 Digital Voltmeter . . . HP 3466A

Set the system center frequency to 2 GHz with an output level of +3 dBm. Use the BNC connector as a probe to measure the RF signals at the various locations indicated by the test points.

Put the center conductor of the probe on the

connection between circuit boards and press the outer conductor ground against the A22 Assembly housing.

Check the power supply inputs to A22A2 and A22A3 if they are suspected of malfunctioning.

NOTE

If A22A2 or A22A3 are defective they must each be replaced as a complete assembly. If a problem exists elsewhere in the A22 Assembly, the entire assembly must be replaced. Refer to the A22 Assembly Repair procedure in Section VIII preceding the service sheets. Section VI contains ordering information for new or restored assemblies,

SERVICE SHEET 8 (Cont'd)

of the amplifier is unity. As the instantaneous base voltage of A3Q6 is increased (by either positive dc level or positive excursions of an AM drive signal) A3CR1 is forward biased and the amplifier gain is dependent on the ratio of A3R3 and the effective resistance of A3CR1. This variable gain is used to compensate for the non-linearity of the A5 Modulator Assembly's input voltage to RF attenuation transfer function.

Pulse Modulation

P

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In the Pulse Modulation mode (HP Model 86631B Auxiliary Section is used in place of a Modulation Section), a PULSE ID logic high (\approx +5 Vdc) turns A3Q1 off which opens A3K1 and thus opens the ALC loop. At the same time, the PULSE ID input biases A2Q1 on, closes A2K1, and connects the Pulse In through A2R9, A2C2, and A2VR1 to the A5 Modulator Assembly. Without a pulse input, the positive bias through A2R8 biases the Modulator for maximum attenuation and reduces the power output to a minimum (>40 dB down). A -10 Vdc input pulse is required to cause the Modulator to exhibit minimum attenuation to the RF Signal.

TROUBLESHOOTING

It is assumed that the Troubleshooting information on Service Sheet 1 was used to isolate a circuit defect to the assemblies shown on the accompanying diagram. Troubleshoot the Reference and ALC Amplifier Assemblies and pulse modulation circuits by using the test equipment and procedures given below.

Test Equipment

Test 1. Check the power supply inputs to the A3 and A10 assemblies at A2XA3 pin 5 (\pm 20V), pin 3 (\pm 5V), and pin 8 (\pm 10V) and A12XA10 pin D (\pm 20V), pin C (\pm 5V), and pin 5(\pm 10V). If the voltages are correct proceed to Test 2. If incorrect, check the continuity of the inputs from the A12 Assembly.

Test 2. Check the Reference Output at P14 Pin E. If the output level is incorrect for the extreme settings of the vernier control or 1 dB Step Attenuator settings (see schematic for levels), proceed to Test 3. If the output is correct, set A4S1 and check the levels at A3TP1 with the VERNIER (or 1 dB Step Attenuator) set to one extreme and then the other. If the output levels are normal, the Gain-Shaping Amplifier or the Modulator Bias Signal resistors are probably defective. Also check the Pulse ID input and the relays. Otherwise, the Difference Amplifier is probably defective.

A22 Frequency Doubler Assembly

SERVICE SHEET 7

NOTE

When a malfunction occurs refer to Section VIII of the Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (Systems Troubleshooting Guide) Then if that information indicates possible problems in the RF section, refer to the Systems troubleshooting information on Service Sheet 1 in this manual This information may be used to isolate the defect to the RF Section another plug-in, or the mainframe. If the problem is in this plug-in refer to Service Sheet 2 for further troubleshooting information.

PRINCIPLES OF OPERATION (A22 FREQUENCY DOUBLER ASSEMBLY)

The input RF signal to the frequency doubler is connected directly to the A22A5 Relay Assembly. In the X1 mode, the 1-1300 MHz signal is switched to the A22A4 Output Detector Assembly and on through A22A4R3 and C2 to the 10 dB Step Attenuator Assembly.

In the X2 mode, a logic high (+12 Vdc) appears on the Doubler Relay Control input. This causes the relay A22A5K1 to switch the input signal (650 to <1300 MHz) to the A22A1 Doubler/Filter Assembly The signal passes through a balun to the bridge rectifier Frequency Doubler, A22A1CR1, The balanced doubler suppresses the fundamental input and odd harmonics while generating a large second harmonic component, A22A1L1 provides a ground return for the dc component of the output signal and R1, R2, and R3 provide RF termination. The output signal passes to the tracking filter. The lead inductance and voltage variable capacitance of the varactor form a series resonant circuit. The Filter Drive input causes the resonant frequency to track the doubled input frequency. The fundamental. odd harmonics, and even harmonics (>4th) are further attenuated but the second harmonic, (≥1300 to <2600 MHz) is passed on to the A22A2 Doubler Amplifier Assembly.

In both the A22A2 and A22A3 amplifiers, the doubled RF signal is amplified by at least 10 dB. The A22A3 output is coupled back through the A22A5 and A22A4 Assemblies and on to the 10 dB Step Attenuator.

The RF signal level is detected and a relative dc level proportional to the RF level is coupled to the inverting differential amplifier in the A4 Detector Amplifier Assembly. The reference diode, which is in the same thermal environment as the detector diode, provides temperature compensation for the detector diode because it is coupled to the non-inverting input of the differential amplifier.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2

A4 Detector Amplifier Assembly A6 1-1300 MHz Amplifier Assembly ♠ SERVICE SHEET 6

SERVICE SHEET 7 (Cont'd)

blice and cables shown on the schematic diagrams Troubleshoot the frequency doubler circuits by using the test equipment and procedures given bolow

Test Equipment

Spectrum Analyzer . . HP 8555A/8552B/140T BNC Connector HP 1250-0118 Digital Voltmeter . . HP 3466A

Set the system center frequency to 2 GHz with an output level of +3 dBm. Use the BNC connector as a probe to measure the RF signals at the various locations indicated by the test points.

Put the center conductor of the probe on the

was used to isolate a circuit defect to the assem. connection between circuit hoards and press the outer conductor ground against the A22 Assembly housing

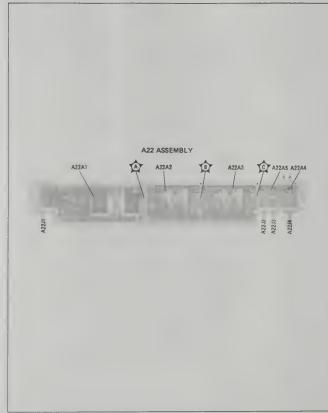
> Check the power supply inputs to A22A2 and A22A3 if they are suspected of malfunctioning.

NOTE

If A22A2 or A22A3 are defective they must each he replaced as a complete assembly. If a problem exists elsewhere in the A22 Assembly the entire assembly must be replaced. Refer to the A22 Assembly Repair procedure in Section VIII preceding the service sheets. Section VI contains ordering information for new or restored assemblies

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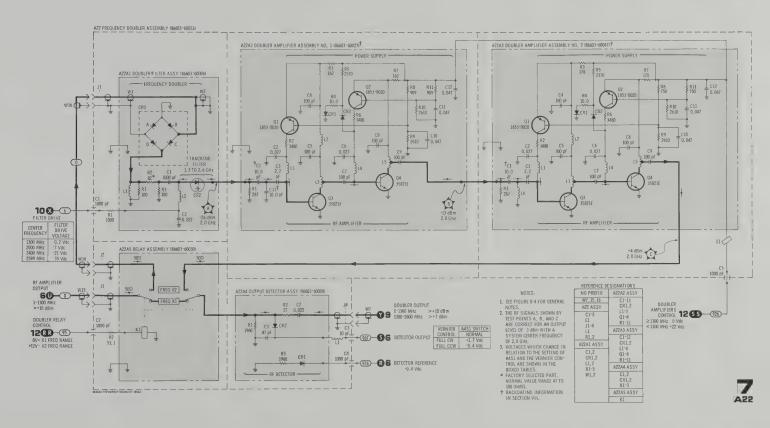


Figure 8-18. A22 Frequency Doubler Subassembly and Test Point Locations

SERVICE SHEET 8 (Cont'd)

Test 3. Check the reference diode A10VR1, and Reference Amplifier A10U1 and their associated components. If the unit responds only to the local control or responds to remote control and not to the VERNIER, check the LCL/RMT input and the relay. If the reference output is incorrect in remote mode only, check the 1 dB Step Attenuator,

relays, transistor switches, and other associated components. Small changes in RF Output level may be traceable to defective components coupled to the 10H input. If it was found that the amplitude modulation level varies with RF Output level, check the components associated with the AM Gain input. If the AM drive signal is reaching the RF Section, verify that it is reaching the A10 Assembly circuitry. Determine which component or part is defective, repair or replace it.

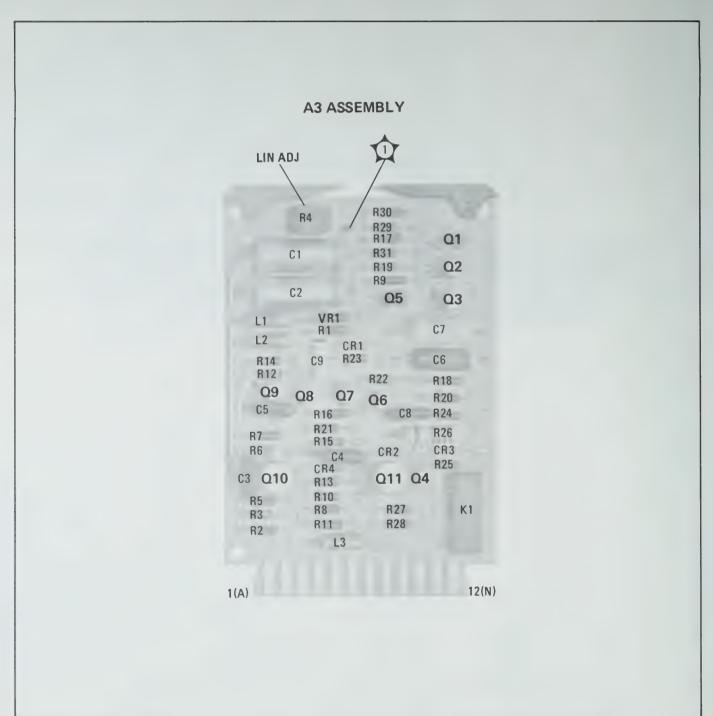


Figure 8-20. A3 ALC Amplifier Assembly Component and Test Point Locations

NOTE

When a malfunction occurs refer to Section VIII of the Model 8660-series mainframe manual to begin troubleshooting (Systems Troubleshooting Guide). If the information then indicates possible problems in the RF Section, refer to the Systems Troubleshooting information which preceeds Service Sheet 1 in this manual This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe, If the problem is in this plug-in, refer to Service Sheet 2 for further troubleshooting information.

PRINCIPLES OF OPERATION

General

The RF Detector signal output from the A4 Detector Amplifier Assembly is coupled into the A3 ALC Amplifier Assembly where it is compared to the reference input. Any difference in dc input levels causes an error output signal (i.e., a change from the loop quiescent state) at the difference amplifier output A3TP1. The error signal is coupled through the Gain-Shaping Amplifier to the A5 Modulator Assembly which controls the RF output level. The change in RF output level is reflected in dc level change at the input to the dc amplifier. The change serves to balance the original error output signal at A3TP1.

A10 Reference Assembly

The Reference Assembly output is coupled to the ALC circuit where it is compared to the Detector Amplifier output. An error signal is generated which causes the RF signal to follow the reference dc level or, in AM mode, a low frequency ac signal which is superimposed on the reference dc output.

A reference dc level is established by A10VR1. This dc level is coupled to the inverting input of A10U1 where (in the +10 dBm range only) a small RF Detector Diode linearity compensation current is added from the 10H input through resistor A10R14. The output of A10U1 passes through a remotely controlled attenuator or an adjustable voltage divider which includes R1 VERNIER Control. This provides fine adjustment of the reference output, i.e., the RF Output level over a 10 dB range.

The Amplitude Modulation drive signal is input at the non-inverting input of A10U1. The AM Gain input is a dc compensation signal which effects the level of the AM drive input. As the VERNIER control is rotated cw. the dc level goes more negative which increases the RF Output level. At the same time a negative change of the AM Gain compensation increases the modulation drive signal attenuation of the AM drive signal input to A10U1. The resulting increase in modulation drive signal at the output of A10U1 tends to keep the percentage modulation level constant with change in RF output level.

In the remote mode, the front panel VERNIER control of the RF output level is inhibited and the 1 dB step attenuator assumes "vernier" control over

SERVICE SHEET 8 (Cont'd)

a 10 dB range. A logic low (<+0.8 Vdc) on the LCL/RMT input lines biases A10Q10 off, which opens the contacts of A10K6 and isolates the VERNIER control. At the same time, A10Q1 is biased on which closes the contacts of A10K5 and enables the 1 dB step attenuator. With no attenuation (RF vernier maximum) the 1A, 2A, 4A, and 8A inputs are all logic lows. Programmed attenuation levels will cause a logic high to appear on the appropriate input. For example, if 1 dB of attenuation is programmed (equivalent to a +2 dB front panel meter reading), a voltage of +5 Vdc will be found on A12XA10 pin J. This voltage biases A10Q9 off. Relay A10K1 opens which causes the reference to be attenuated through A10R21 and A10R22 (which is coupled to ground through A10Q8). When A10Q9 is turned off, bias current is supplied through A10R20 from the negative supply to turn A10Q8 on Transistor A10Q8 is baised through the base-to-collector junction instead of the normal base-to-emitter junction.

Each step of attenuation is operated in the same manner. The values of the resistors in the voltage divider network are weighted for greater attenuation of voltage output to the ALC circuits as the programmed attenuation levels are increased.

ALC Amplifier Assembly

The Detector Amplifier output, which is proportional to the RF output level, is compared to the Reference output in the ALC Amplifier Assembly.

The detector signal is coupled to the non-inverting input of the discrete operational amplifier (A3Q10, A3Q9, and associated components) while the reference input is coupled to the inverting input. Under normal operating conditions a change in reference input causes an error output signal at A3TP1. This signal passes through the Gain-Shaping Amplifier where it is coupled to the A5 Modulator Assembly. This change in Modulation Bias Signal causes the RF output to change. The change is reflected in the Detector Amplifier input to the ALC loop. This change serves to balance the error signal at A3TP1 and a new quiescent voltage is established. In a similar fashion, the change in RF output loading or a change in signal level input from the Frequency Extension Module is compensated for in the ALC loop. For example, a decrease in output level due to increased loading causes a positive change in the Detector Amplifier output to the ALC Amplifier. The resultant change in Modulator Bias Signal is negative which decreases the A5 Modulator Assembly Attenuation of the RF Signal and subsequently increases the RF output level.

At <10 MHz and >1300 MHz, a logic high (>+4.0 Vdc) at the ALC BW Control input biases A3Q5 off, A3Q2 is biased off, and A3Q3 is turned on. A3C6 is now coupled to ground which effectively reduces the bandwidth of the ALC loop. This occurs so the ALC loop does not respond to individual cyclic variations in the RF Signal but rather to the relatively long term peak output of the RF Detector at center frequencies <10 MHz. At or above 1300 MHz, the reduced bandwidth ensures ALC loop stability.

Gain-Shaping Amplifier

The Gain-Shaping Amplifier is a discrete operational amplifier made up of A3Q7, A3Q8, A3Q6, A3Q11, A3Q4, and their associated components. The gain-shaping component is A3CR1. When A3CR1 is reverse biased the gain

SERVICE SHEET 8 (Cont'd)

of the amplifier is unity. As the instantaneous base voltage of A3Q6 is increased (by either positive dc level or positive excursions of an AM drive signal) A3CR1 is forward biased and the amplifier gain is dependent on the ratio of A3R3 and the effective resistance of A3CR1. This variable gain is used to compensate for the non-linearity of the A5 Modulator Assembly's input voltage to RF attenuation transfer function.

Pulse Modulation

In the Pulse Modulation mode (HP Model 86631B Auxiliary Section is used in place of a Modulation Section), a PULSE ID logic high (≈+5 Vdc) turns A3Q1 off which opens A3K1 and thus opens the ALC loop. At the same time, the PULSE ID input biases A2Q1 on, closes A2K1, and connects the Pulse In through A2R9, A2C2, and A2VR1 to the A5 Modulator Assembly. Without a pulse input, the positive bias through A2R8 biases the Modulator for maximum attenuation and reduces the power output to a minimum (>40 dB down). A -10 Vdc input pulse is required to cause the Moduator to exhibit minimum attenuation to the RF Signal.

TROUBLESHOOTING

It is assumed that the Troubleshooting information on Service Sheet 1 was used to isolate a circuit defect to the assemblies shown on the accompanying diagram. Troubleshoot the Reference and ALC Amplifier Assemblies and pulse modulation circuits by using the test equipment and procedures given

Test Equipment

Test 1. Check the power supply inputs to the A3 and A10 assemblies at A2XA3 pin 5 (+20V), pin 3 (+5V), and pin 8 (-10V) and A12XA10 pin D (+20V), pin C (+5V), and pin 5(-10V). If the voltages are correct proceed to Test 2. If incorrect, check the continuity of the inputs from the A12 Assembly

Test 2. Check the Reference Output at P14 Pin E. If the output level is incorrect for the extreme settings of the vernier control or 1 dB Step Attenuator settings (see schematic for levels), proceed to Test 3. If the output is correct, set A4S1 and check the levels at A3TP1 with the VERNIER (or 1 dB Step Attenuator) set to one extreme and then the other. If the output levels are normal, the Gain-Shaping Amplifier or the Modulator Bias Signal resistors are probably defective. Also check the Pulse ID input and the relays. Otherwise, the Difference Amplifier is probably defective.

> A22 Frequency Doubler Assembly SERVICE SHEET 7

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SERVICE SHEET 8 (Cont'd)

Test 3. Check the reference diode A10VR1, and Reference Amplifier A10U1 and their associated the VERNIER, check the LCL/RMT input and the relay. If the reference output is incorrect in remote mode only, check the 1 dB Step Attenuator, or part is defective, repair or replace it.

relays, transistor switches, and other associated components. Small changes in RF Output level may be traceable to defective components coupled to the 10H input. If it was found that the amplitude modulation level varies with RF Output components. If the unit responds only to the local level, check the components associated with the control or responds to remote control and not to AM Gain input. If the AM drive signal is reaching the RF Section, verify that it is reaching the A10 Assembly circuitry. Determine which component

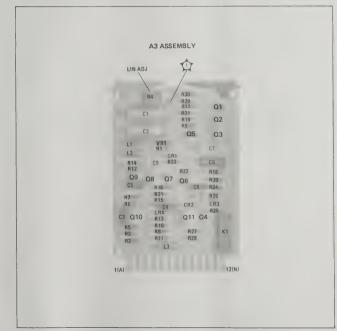


Figure 8-20. A3 ALC Amplifier Assembly Component and Test Point Locations

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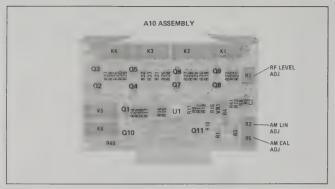


Figure 8-21. A10 Reference Assembly Component Locations

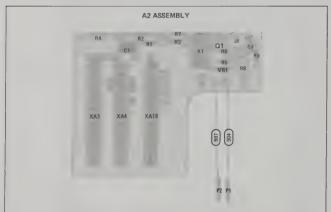
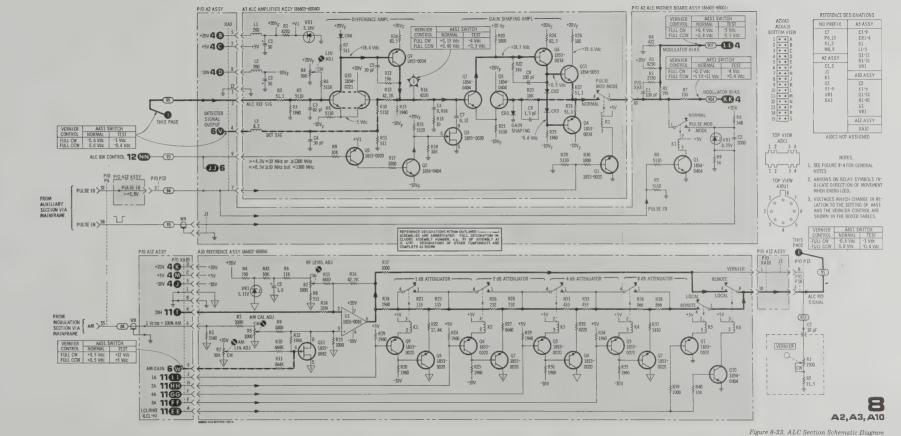


Figure 8-22. A2 ALC Mother Board Assembly Component Locations



Service Model 86603A

SERVICE SHEET 9

NOTE

When a malfunction occurs, refer to Section VIII of the Model 8660-series mainframe manual to begin troubleshooting (System Troubleshooting Guide). If the information then indicates possible problems in the RF Section, refer to the Systems Troubleshooting information in Service Sheet 1 of this manual. This information may be used to isolate the defect to the RF Section, another plugin or the mainframe. If the problem is in this plug-in refer to Service Sheet 2 for further troubleshooting information before returning here.

PRINCIPLES OF OPERATION

Logic high inputs (>+2.0 Vdc) from the A11 Logic Board Assembly will cause the driver transistors to supply current to switch the appropriate attenuator section in the A13 Attenuator Assembly. For example, if 10 dB of attenuation is desired, the 10L input goes high, A9Q15 is biased on; A9Q11 is also biased on and supplies driving current to switch A13K1. The relay arms all drop down into the lower position. The RF Signal flow is now through attenuator section AT1 (10 dB). The two lower relay arms provide a latching function for the relay. This means that until a drive current of the correct polarity is input to the A9 Attenuator Drive Assembly, the relay is latched in its present state. Also, no current flows after the switching has been completed. A9R6 and A9VR1 provide the proper bias level for the input transistors so they will respond correctly to the inputs.

The other attenuator sections function the same way as the 10 dB section. However, the 80 dB section actually uses two 40 dB sections in parallel.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2 was used to isolate a circuit defect to the assemblies shown on the accompanying diagram. Troubleshoot the Attenuator and Attenuator Driver Assemblies using the test equipment and procedures given below.

Test Equipment

Digital Voltmeter. HP 3466A

The malfunction may be isolated to either the A13 or A9 Assemblies by measuring the 10D, 20D, 40D, and 80D control lines and determining if they are correct. If the problem is in the A13 Assembly DO NOT attempt to repair it. It is not a field repairable unit.

NOTE

A13 Assembly is not a field repairable unit. If a problem occurs in this assembly, DO NOT attempt to repair it.

DC voltage checks should be sufficient to quickly isolate a defective component in the A9 Assembly. Remember, current flows through the drive transistors only until latching of the relays in A13 is completed.

Summing Amplifiers

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There are three summing amplifiers in this Digital-to-Analog Converter. In order to gain an understanding of how each works, a basic summing amplifier is first explained. Then, information which applies to each individually is included.

General. Each input to a summing amplifier is independent. The output due to each input is the product of the voltage input and the individual gain for that input. The total summing amplifier output is determined by the summation of the output due to each input. For example, in the Summing Amplifier shown below, the output voltage due to each input is determined by the following equation:

$$V_o = V_{in} \left(-\frac{R_f}{R_{in}} \right)$$

where

Vo is the output voltage

V_{in} is the input voltage

 R_{f} is the feedback resistance

R_{in} is the input resistance

$$\left(-\frac{R_f}{R_{in}}\right)$$
 is the gain

The negative gain implies 180° phase shift. The same formula is applicable for offset voltage inputs.

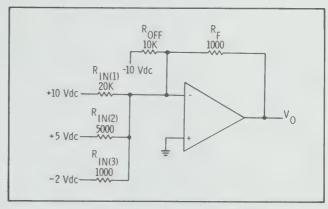


Figure 8-26. Summing Amplifier

The offset voltage as shown in the figure is:

$$V_{\text{off}} = (-10 \text{ Vdc}) \left(-\frac{1000}{10 \text{ K}} \right)$$

$$V_{\text{off}} = (-10 \text{ Vdc}) \left(-\frac{1}{10} \right)$$

$$V_{\text{off}} = +1 \text{ Vdc}$$

NOTE

When a malfunction occurs, refer to Section VIII of the Model 8660-series mainframe manual to begin troubleshooting (System Troubleshooting Guide). If the information then indicates possible problems in the RF Section, refer to the Systems Troubleshooting information in Service Sheet 1 of this manual. This information may be used to isolate the defect to the RF Section another plugin or the mainframe. If the problem is in this plug-in refer to Service Sheet 2 for further troubleshooting information before returning here,

PRINCIPLES OF OPERATION

10L input goes high, A9Q15 is biased on; A9Q11 is repairable unit. also biased on and supplies driving current to switch A13K1. The relay arms all drop down into the lower position. The RF Signal flow is now through attenuator section AT1 (10 dB). The two lower relay arms provide a latching function for the relay. This means that until a drive current of the correct polarity is input to the A9 Attenuator will respond correctly to the inputs.

The other attenuator sections function the same way as the 10 dB section. However, the 80 dB section actually uses two 40 dB sections in parallel.

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TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 2 was used to isolate a circuit defect to the assemblies shown on the accompanying diagram. Troubleshoot the Attenuator and Attenuator Driver Assemblies using the test equipment and procedures given below.

Digital Voltmeter. HP 3466A

Logic high inputs (>+2.0 Vdc) from the A11 Logic The malfunction may be isolated to either the A13 Board Assembly will cause the driver transistors to or A9 Assemblies by measuring the 10D, 20D, supply current to switch the appropriate attenu- 40D, and 80D control lines and determining if they ator section in the A13 Attenuator Assembly. For are correct. If the problem is in the A13 Assembly example, if 10 dB of attenuation is desired, the DO NOT attempt to repair it. It is not a field

NOTE

A13 Assembly is not a field repairable unit. If a problem occurs in this assembly, DO NOT attempt to repair it.

Drive Assembly, the relay is latched in its present DC voltage checks should be sufficient to quickly state. Also, no current flows after the switching has isolate a defective component in the A9 Assembly. been completed. A9R6 and A9VR1 provide the Remember, current flows through the drive transisproper bias level for the input transistors so they tors only until latching of the relays in A13 is completed.

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Model 86603A Service

P/0 P6

FROM MAIN-



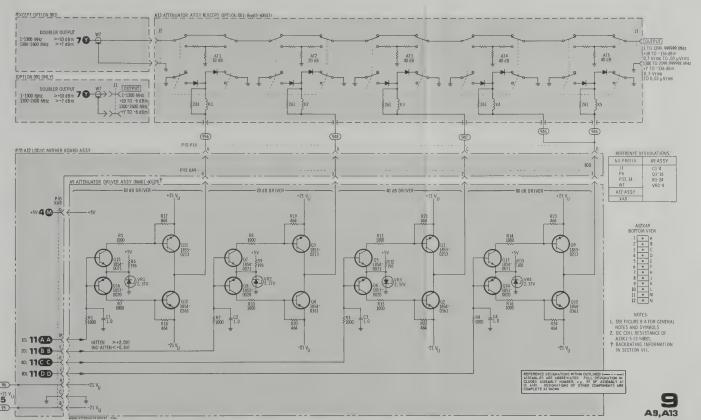


Figure 8-24, A9 Attenuator Driver Assembly Component Locations

Figure 8-25. Attenuator Section Schematic Diagram

SERVICE SHEET 10 (Cont'd)

The input and output voltage and input gains are shown in the following table.

V _{in} (Vdc)	Gain	V _o
-10 +10 +5 -2	$ \begin{array}{r} -0.1 \\ -0.05 \\ -0.2 \\ -1.0 \end{array} $	+1.0 -0.5 -1.0 +2.0

The amplifier output is equal to the sum of the outputs or +1.5 Vdc. If, for instance, the offset voltage is set to zero the offset input contribution to the amplifier output would be:

$$V_o = (0 \text{ Vdc}) \left(-\frac{1000}{10\text{K}}\right)$$
$$V_o = 0$$

The amplifier output would now be +0.5 Vdc.

Final Summing Amplifier. This circuit operates almost the same as a normal summing amplifier except for the addition of Q2. Q2 provides the additional voltage range needed to drive the tracking generator circuit. The phase inversion is also due to Q2.

Of the seven inputs, the six from the inverters set the voltage for each 200 MHz step. At each step, only one of the six inputs from the hex inverters is high (+5 Vdc). The seventh input (from the Increment Summing Amplifier) controls the voltage offset for the 40 MHz steps.

Increment Summing Amplifier. The output voltage of the Increment Summing Amplifier depends on an offset input (through R26) and the three inputs from the Fine Tuning Summing Amplifier which are selected by the eighth digit digital inputs. At the even 200 MHz steps, all the D8 inputs are low (<+0.8 Vdc). This causes the selected inputs to the Increment Voltage Generator to be at ground potential. Therefore, the output is dependent only on the offset input. As shown in the Eighth Digit Digital Inputs table, the different inputs are activated at the various 40 MHz steps across each 200 MHz step. A high logic input causes the hex inverter output to the resistor divider network to float. This occurs because the inverters are open collector types. When this happens, the output from the Unity Gain Inverter is coupled through the series resistors (either 8000, 4000, or 2000 ohms) to the Increment Summing

Amplifier. The amplifier output is now dependent on the sum of the offset voltage and the voltage change due to the selected inputs.

Fine Tune Summing Amplifier. The output of this amplifier is unique for each 200 MHz segment. Like the Final Summing Amplifier, the inputs from the inverters control the voltage output for each segment. The seventh input, the 1300 MHz Adjust (offset) sets the voltage for the 1300 MHz to <1400 MHz segment. The adjustable inputs are made at a common 40 MHz step (same eighth digit digital input for each 200 MHz step).

TROUBLESHOOTING

It is assumed that the troubleshooting information in Service Sheet 3 was used to isolate a circuit defect to the A21 Assembly. Troubleshoot the circuits using the test equipment and information which follows.

Test Equipment

Digital Voltmeter. HP 3466A

Before proceeding with the troubleshooting information, check the power supply inputs to the assembly.

Quickly step through the frequencies from 0 to 2400 MHz in 100 MHz steps. The only voltage change at the High Pass Filter Switch output should occur when switching between frequencies ≥100 MHz and <100 MHz.

To check the Filter Drive output, set the center frequency to 1300 MHz. Note the output voltage at TP1. Increase the center frequency to 1320 MHz and verify a small negative voltage increase. Increase the frequency in 40 MHz steps to 2560 MHz. A nonlinear negative increase in voltage should occur at each step.

A 200 MHz step which is completely incorrect is probably due to a malfunction or incorrect adjustment in the U1, U2 or U3 circuits or their associated components. An individual 40 MHz step which is incorrect is probably due to a malfunction in U7 or R16. If the 200 MHz steps are correct but the 40 MHz steps are offset within one 200 MHz step U1, U3, U4, U6 (C or D) or an associated component is probably misadjusted or defective. If the 200 MHz steps are correct but all the 40 MHz steps are offset at all steps, U6 (A or B) or an associated component is probably defective. See Filter Driver Adjustment procedure in Section V for correct output voltages.

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C7 U5

52 **Q2** 63 C13 C14

L1

SERVICE SHEET 11 (Cont'd)

Logic Assembly Inputs Versus Outputs

Prog	gramm	ed Atte	enuatio	n Inpu	ıt	ОИТРИТ	L	ogic As	ssembly	Outp	ut
Decimal		2-	Digit B	CD		RANGE					Over- range
(dB)	100	80	40	20	10	Decimal (dBm)	80 L	40L	20 L	10 L	10H
0	L	L	L	L	L	+10	L	L	L	L	Н
10	L	L	L	L	Н	0	L	L	L	Ł	L
20	L	L	L	Н	L	-10	L	L	L	Н	L
30	L	L	L	Н	Н	-20	L	L	Н	L	L
40	L	L	Н	L	L	-30	L	L	Н	Н	L
50	L	L	Н	L	Н	-40	L	Н	L	L	L
60	L	L	Н	Н	L	-50	L	Н	L	Н	L
70	L	L	Н	Н	Н	-60	L	Н	Н	L	L
80	L	Н	L	L	L	-70	L	Н	Н	Н	L
90	L	Н	L	L	Н	-80	Н	L	L	L	L
100	Н	L	L	L	L	-90	Н	L	L	Н	L
110	Н	L	L	L	Н	-100	Н	L	Н	L	L
120	Н	L	L	Н	L	-110	Н	L	Н	Н	L
130	Н	L	L	Н	Н	-120	Н	Н	L	L	L
140	Н	L	Н	L	L	-130	Н	Н	L	Н	L
150*	Н	L	Н	L	Н	-140*	Н	Н	Н	L	L

^{*} For safety purposes, the shift registers are set for 150 dB attenuation upon initiation the remote mode of operation.

BCD-To-Binary Converter

	In	put			Output	
100	80	40	20	80	40	20
L	L	L	L	L	L	L
L	L	L	Н	L	L	Н
L	L	Н	L	L	Н	L
L	L	Н	Н	L	Н	Н
L	Н	L	L	Н	L	L
Н	L	L	L	Н	L	Н
Н	L	L	Н	Н	Н	L
Н	L	Н	L	Н	Н	Н

NOTE

When a malfunction occurs, refer to Section VIII of the Model 8660-series mainframe manual to begin troubleshooting (Systems Troubleshooting Guide). If the information then indicates possible problems in the RF Section, refer to the Systems Troubleshooting information in Service Sheet 1 of this manual. This information is used to isolate the defect to the RF Section, another plug-in, or the mainframe If the problem is in this plug-in, refer to Service Sheet 2 for preliminary troubleshooting information.

PRINCIPLES OF OPERATION

General

The A21 Filter Driver Assembly provides two independent filter control functions. The first is a simple switching circuit. The High Pass Filter Switch output switches a 50 MHz high pass filter into the 1-1300 MHz signal path at system center frequencies greater or equal to 100 MHz. The second circuit performs digital-to-analog conversion of center frequency and voltage. The Filter Drive output voltage controls the frequency of a tracking band pass filter which is found in the A22 Frequency Doubler Assembly.

The digital input to the A21 Assembly is dependent on the center frequency eighth, ninth, and tenth digits (10 and 100 MHz, and 1 GHz respectively). Below 1300 MHz, the selected center frequency and the digital input are the same. Bear in mind that at center frequencies of 1300 MHz or above (as shown on the table and on the schematics), the digital control inputs are one half the center frequency.

The Frequency Decoder circuits respond with an output whenever the selected

_			Los	ic Cor	itrol			OUTPUTS					
Center Frequency	PreDoubled Frequency		Inputs				U3B	U3A BCD-to-Dec. De			c. Dec	oder	
(MHz)	(MHz)	D10	D9-8	D9-4	D9-2	D9-1	(12)	(11)	(10)	9	8	7	
0	*	L	L	L	L	L	Н	Н	L	Н	Н	Н	
100	*	L	L	L	L	Н	Н	Н	Н	H	H	Н	
1000	*	H	L	L	L	L	H	Н	L	Н	H	H	
1100	*	H	L	L	L	Н	Н	L	Н	Н	Н	Н	
1300	650	L	L	Н	Н	L	H	Н	Н	H	Н	H	
1400	700	L	L	H	H	Н	H	H	H	Н	Н	L	
1600	800	L	Н	L	L	L	H	Н	H	Н	L	Н	
1800	900	L	H	L	L	Н	H	Н	Н	L	H	H	
2000	1000	H	L	L	L	L	Н	Н	L	Н	Н	Н	
2200	1100	H	L	L	L	H	Н	L	H	Н	H	Н	
2400	1200	Н	L	L	H	L	L	Н	H ·	H	Н	H	

*Output frequency is not doubled at center frequencies < 1300 MHz.

SERVICE SHEET 10 (Cont'd)

center frequency is within a segment controlled by the A21 Assembly circuits. The outputs are coupled directly or through inverters to the High Pass Filter Switch and the Filter Drive circuits.

Frequency Decoders and Hex Inverters

Each of the one-of-six Frequency Decoder outputs is coupled in parallel to two CMOS hex inverters. The U2 inverter outputs provide either 0 Vdc or a reference +5 Vdc to six of the seven Final Summing Amplifier inputs. The A21U4 inverter outputs provide 0 Vdc or the +5 Vdc reference to six of the seven Fine Tune Summing Amplifier inputs.

High Pass Filter Switch

The High Pass Filter Switch output is controlled by the D10 digital control line and the inverted "0" output from the BCD-to-Decimal Decoder. At center frequencies equal to or greater than 1 GHz, the level on the D10 line holds the HPF Switch output low (\$\approx - 8 Vdc). At center frequencies less than 1 GHz, control is passed to the inverted "0" control line. Only at center frequencies <100 MHz does the combination of inputs cause the output to go high (\$\approx +10 Vdc). At these frequencies the 50 MHz High Pass Filter is removed from the RF signal path.

Filter Drive Circuits

The Filter Drive digital-to-analog converter is made up of three summing amplifiers and a programmable resistor divider network. The Final Summing Amplifier's adjustable inputs control the 200 MHz steps (1400, 1600, 1800 MHz, etc.). Because the frequency-to-voltage curve is logarithmic, each adjustment is made individually.

The Fine Tune Summing Amplifier provides an output equivalent to 200 MHz steps into which the 40 MHz steps are inserted. The Increment Voltage Divider Network is connected between the output of the Fine Tune Summing Amplifier and the input to the Increment Summing Amplifier. This network allows the linear interpolation of the 40 MHz steps between the 200 MHz steps because the eighth digit digital input controls the voltage level actually coupled to the Increment Summing Amplifier.

Eighth Digit Digital Inputs

Frequency	Predoubled Frequency (MHz)							
(MHz)		D8-8	D8-4	D8-2				
0	0	L	L	L				
40	20	L	L	Н				
80	40	L	H	L				
120	60	L	H	Н				
160	80	H	L	L				

*The low inputs (L) are at ground potential. The high inputs (H) are normally one-half the voltage found on pin 8 of U6C.

SERVICE SHEET 10 (Cont'd)

Summing Amplifiers

There are three summing amplifiers in this Digital-to-Analog Converter. In order to gain an understanding of how each works, a basic summing amplifier is first explained. Then, information which applies to each individually is included.

General. Each input to a summing amplifier is independent. The output due to each input is the product of the voltage input and the individual gain for that input. The total summing amplifier output is determined by the summation of the output due to each input. For example, in the Summing Amplifier shown below, the output voltage due to each input is determined by the following equation:

$$V_o = V_{in} \left(-\frac{R_f}{R_{in}} \right)$$

V_ is the output voltage

V: is the input voltage

R. is the feedback resistance

Ria is the input resistance

$$\left(-\frac{R_f}{R_{in}}\right)$$
 is the gain

The negative gain implies 180° phase shift. The same formula is applicable for offset voltage inputs.

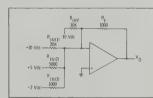


Figure 8-26. Summing Amplifier

The offset voltage as shown in the figure is:

$$V_{\text{off}} = (-10 \text{ Vdc}) \left(-\frac{1000}{10 \text{ K}} \right)$$

 $V_{\text{off}} = (-10 \text{ Vdc}) \left(-\frac{1}{10} \right)$

A9 Attenuator Driver Assembly A13 Attenuator Assembly **▲** SERVICE SHEET 9

SERVICE SHEET 10 (Cont'd)

Service

The input and output voltage and input gains are shown in the following table.

V _{in} (Vdc)	Gain	V _o
-10	-0.1	+1.0
+10	-0.05	-0.5
+5	-0.2	-1.0
-2	-1.0	+2.0

The amplifier output is equal to the sum of the outputs or +1.5 Vdc. If for instance the offset voltage is set to zero the offset input contribution to the amplifier output would be:

$$V_o = (0 \text{ Vdc}) \left(-\frac{1000}{10\text{K}}\right)$$

 $V_o = 0$

The amplifier output would now be +0.5 Vdc.

Final Summing Amplifier. This circuit operates almost the same as a normal summing amplifier except for the addition of Q2, Q2 provides the additional voltage range needed to drive the tracking generator circuit. The phase inversion is also due to Q2.

Of the seven inputs, the six from the inverters set the voltage for each 200 MHz step. At each step, only one of the six inputs from the hex inverters is high (+5 Vdc). The seventh input (from the Increment Summing Amplifier) controls the voltage offset for the 40 MHz steps.

Increment Summing Amplifier. The output voltage of the Increment Summing Amplifier depends on an offset input (through R.26) and the three inputs from the Fine Tuning Summing Amplifier which are selected by the eighth digit digital inputs. At the even 200 MHz steps, all the D8 inputs are low (<+0.8 Vdc). This causes the selected inputs to the Increment Voltage Generator to be at ground potential. Therefore, the output is ated components. An individual 40 MHz step which dependent only on the offset input. As shown in the Eighth Digit Digital Inputs table, the different inputs are activated at the various 40 MHz steps across each 200 MHz step. A high logic input U1, U3, U4, U6 (C or D) or an associated comcauses the hex inverter output to the resistor ponent is probably misadjusted or defective. If the divider network to float. This occurs because the inverters are open collector types. When this happens, the output from the Unity Gain Inverter is coupled through the series resistors (either 8000. 4000, or 2000 ohms) to the Increment Summing

Amplifier. The amplifier output is now dependent on the sum of the offset voltage and the voltage change due to the selected inputs.

Model 86603 A

Fine Tune Summing Amplifier. The output of this amplifier is unique for each 200 MHz segment. Like the Final Summing Amplifier, the inputs from the inverters control the voltage output for each segment. The seventh input, the 1300 MHz Adjust (offset) sets the voltage for the 1300 MHz to <1400 MHz segment. The adjustable inputs are made at a common 40 MHz step (same eighth digit digital input for each 200 MHz step).

TROUBLESHOOTING

It is assumed that the troubleshooting information in Service Sheet 3 was used to isolate a circuit defect to the A21 Assembly, Troubleshoot the circuits using the test equipment and information which follows.

Digital Voltmeter. HP 3466A

Before proceeding with the troubleshooting information, check the power supply inputs to the assembly.

Quickly step through the frequencies from 0 to 2400 MHz in 100 MHz steps. The only voltage change at the High Pass Filter Switch output should occur when switching between frequencies

To check the Filter Drive output, set the center frequency to 1300 MHz. Note the output voltage at TP1, Increase the center frequency to 1320 MHz and verify a small negative voltage increase. Increase the frequency in 40 MHz steps to 2560 MHz. A nonlinear negative increase in voltage should occur at each step.

A 200 MHz step which is completely incorrect is probably due to a malfunction or incorrect adjustment in the U1, U2 or U3 circuits or their associis incorrect is probably due to a malfunction in U7 or R16. If the 200 MHz steps are correct but the 40 MHz steps are offset within one 200 MHz step 200 MHz steps are correct but all the 40 MHz steps are offset at all steps. U6 (A or B) or an associated component is probably defective. See Filter Driver Adjustment procedure in Section V for correct

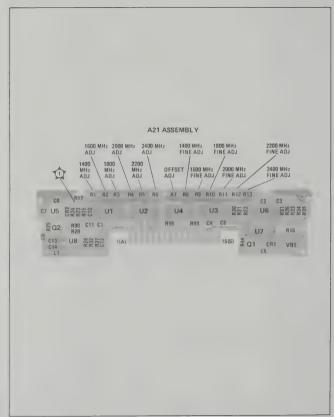
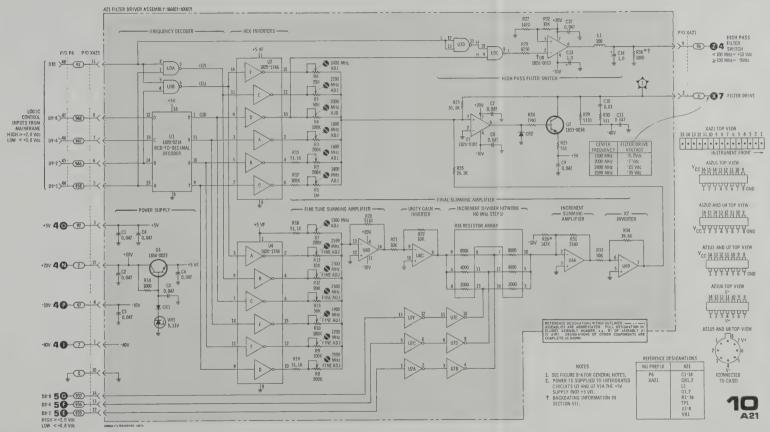


Figure 8-27. A21 Filter Driver Assembly Component and Test Point Locations



Service Model 86603A

SERVICE SHEET 11 (Cont'd)

Full Adder

			Inputs			Out	puts	
A ₄	A ₃	A ₂	A ₁	C ₀ , B ₂ , B ₃ , B ₄	Σ4	Σ3	Σ_{2}	Σ1
80	40	20	10	Over-range	80	40	20	10
L	L	L	L	L	L	L	L	L
L	L	L	Н	Н	L	L	L	L
L	L	Н	L	Н	L	L	L	Н
L	L	Н	Н	Н	L	L	Н	L
L	Н	L	L	Н	L	L	Н	Н
L	Н	L	Н	Н	L	Н	\mathbf{L}	L
L	Н	Н	L	Н	L	Н	L	Н
L	Н	H	Н	Н	L	H	Н	L
Н	L	L	L	Н	L	Н	Н	Н
Н	L	L	Н	Н	H	L	L	L
Н	L	Н	L	Н	Н	L	\mathbf{L}	H
Н	L	_H	Н	Н	H	L	Н	L
Н	Н	L	L	Н	Н	L	Н	Н
Н	Н	L	Н	Н	Н	Н	L	L
Н	Н	Н	L	Н	Н	Н	L	Н
Н	Н	Н	Н	Н	Н	Н	Н	L

Local Remote Multiplex

The LCL/RMT input is a logic low in the remote mode. This enables the gates which are connected to the remote attenuation inputs (Full Adder and Over-range) so the remote signals drive the 10 dB Step Attenuator. At the same time logic inputs from the OUTPUT RANGE switch are inhibited.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 3 was used to isolate a circuit defect to the assembly shown on the accompanying diagram. Troubleshoot the Logic Assembly by using the test equipment and procedures given below.

Test Equipment

Digital Voltmeter . . . HP 3466A

If the problem is evident only in the local mode of operation, check the OUTPUT RANGE switch, continuity of the connections to the A11 assembly, and the Local/Remote Multiplexer. Refer to

the table showing the OUTPUT RANGE switch output. If the defect is evident only in the remote mode of operation, check the shift registers, the BCD-to-Binary Decoder, the Full Adder, and the Local/Remote Multiplexer for proper operation. Use the tables showing inputs versus outputs as a tool to isolate the defective component.

If the defect is evident in both the Local and Remote modes, the Local/Remote Multiplexer or an associated component is probably defective.

NOTE

If the inputs and outputs of the A11 Logic Assembly are correct, check the 10 dB Step Attenuator (Service Sheet 6) in all ranges, the 10 dB Attenuator in the A4 Detector Amplifier Assembly, and the 1 dB Step Attenuator in the A10 Reference Assembly (also the 10H inputs and associated components). Also, check the 1 dB and 10 dB Step Attenuator outputs with attenuation inputs of 1, 2, 4, and 8 dB and 10, 20, 40, and 80 dB.

SERVICE SHEET 12 (Cont'd)

A 20 Assembly Inputs and Outputs

Center	Inp	outs	Control Outputs				
Frequency	DBL-L	Code 1	Doubler Amplifiers	ALC BW	Doubler Relay		
<10 MHz	Н	Н	0 Vdc	>+4.0 Vdc	0 Vdc		
≥10 MHz but <1300 MHz	Н	L	0 Vdc	<+0.3 Vdc	0 Vdc		
≤1300 MHz	L	L	+22 Vdc	>+4.0 Vdc	+12 Vdc		
*H = >+2.0 Vdc	Γ = <-	-0.8 Vdc					

Power Supply Switch. When A20Q2 is biased "on," the drive current to the regulator transistors (both internal and external to A20U1) is removed. This causes the regulator output to go to ground potential. This occurs only with the DBL-L input high (>+2.0 Vdc).

Relay Driver. When the system is operating in the frequency doubling mode, the DBL-L input is low. Therefore, A20Q3 is biased off, A20Q4 is biased on, and approximately +12 Vdc appears at the Doubler Relay Control output.

ALC Bandwidth Control. At center frequencies <10 MHz, the Code 1 input is high. A20Q5 is biased on, A20Q6 is biased off, and the ALC BW Control output increases until it is limited by A20VR2 ($\approx+5$ Vdc). At center frequencies ≥1300 MHz, the override voltage from the Doubler Relay Control output (connected to A20Q5 through A20CR2 and A20R16) cancels the effect of the Code 1 low input. The ALC BW Control again increases to $\approx+5$ Vdc.

Frequency Doubler Test Switch (Except Option 003 Instruments)

When used in an $8660 \, \mathrm{C}$ mainframe, the Frequency Doubler Test Switch S1 should be left in the $8660 \, \mathrm{C}$ position. The other two switch positions are strictly for test purposes. The diode CR1 isolates the DBL-L input from ground in the $8660 \, \mathrm{A/B} \, \mathrm{X2}$ position.

The grounded OP-2 output (in the 8660C position of S2) indicates to the mainframe DCU that the Center frequency limit of the RF Section is 2600 MHz. In the other positions, a limit of 1300 MHz is indicated by the grounded OP-1 output.

Option 003 Instruments

Option 003 instruments are intended to be used with 8660A or 8660B mainframes to provide the frequency doubling capability. The Frequency Doubler Test Switch, A24S1 should be set to the 8660A/B position. The OP-1 output to the mainframe is grounded indicating a maximum frequency of 1300 MHz. In the doubling mode, the mainframe center frequency readout indicates one-half the actual output frequency.

NOTE

When a malfunction occurs, refer to Section VIII of the Model 8660-series mainframe manual to begin troubleshooting (Systems Troubleshooting Guide). If the information then indicates possible problems in the RF Section, refer to the Systems Troubleshooting information in Service Sheet I of this manual. This information is used to isolate the defect to the RF Section, another plug-in, or the mainframe. If the problem is in this plug-in, refer to Service Sheet 2 for preliminary troubleshooting information.

PRINCIPLES OF OPERATION

Local (Front panel) Control

The front panel OUTPUT RANGE switch provides a binary coded hexadecimal input (1F, 2F, 4F, 8F) and an over range input (1H) to the Al1 Assembly in the local mode. The LCL/RMT input is logic high (>+1.8 Vdc) which causes the switch inputs to be gated directly to the outputs to the attenuator driver circuits and the 10H output. The following table shows the logic states of the inputs from the OUTPUT RANGE switch SI. The input signals are all active highs (attenuation) as are the outputs.

Local Inputs to A11 Logic Assembly

	Over-Range Input*
1F	1H
L	L
L	H
H	H
L	H
H	H
L	H
H	H
L	H
H	H
L	Н
H	H
L	H
H	H
L	H
H	H
	L

^{*}L = < +0.8 Vdc; H = > +1.3 Vdc

SERVICE SHEET 11 (Cont'd)

Remote Operation

In the remote mode, 3 digits of BCD attenuation information are clocked into the A11 Assembly Shift Registers from the System mainframe. On the ATTN CLK input, a series of 10 pulses are received at pin K. These pulses are coupled to the trigger (T) input to the shift registers. The data input, which is synchronized with the pulses, contain no usable information for the first seven pulses. On the eighth pulse, units information is clocked into the left-handed column of registers with logic highs indicating data ones and lows indicating zeroes. On the ninth pulse, the units information is shifted to the center column of registers while tens information is entered into the left hand registers. On the tenth pulse, the units word is shifted into and stored in the right hand column, the tens information in the center registers, and the hundreds information in the left registers.

The BCD information stored in the units registers is coupled to the 1 dB Step Attenuator on the A10 Reference Assembly. (In local mode these outputs are not used. The VERNIER control is used for fine control of output level.)

The other two digits of BCD information are coupled to the BCD-to-Binary Decoder. The binary tens line actually bypasses the decoder because it expresses odd or even value in either the BCD or binary coded hexadecimal format. The second digit (20, 40 and 80) and third digit (100) in BCD format are output from the BCD-to-Binary Decoder in a 20, 40, and 80 binary format. With the tens level, these outputs are binary coded hexadecimal. In order to obtain the over-range output (10H), the 10, 20, 40 and 80 coded signals are inverted and coupled to a four input nand gate. The nand gate (over-range) output is low only with zero input attenuation (i.e., all the BCD-to-Binary Decoder output lines are low). The over-range level is coupled to A11 U5C and therefore to the 10H output. It is also coupled to the Full Adder along with the 10, 20, 40, and 80 lines. The inputs to the adder are connected so a value of 10 is subtracted from the input with the Over-Range inactive (high); when the over-range line is low the output follows the input directly. The following tables express the assembly inputs and outputs, the BCD-to-Binary converter inputs and outputs, and the Full Adder inputs and outputs. In each case, a level of >+2.0 Vdc is a logic high and <+0.8 Vdc is logic low.

SERVICE SHEET 11 (Copt'd)

Logic Assembly Innuts Versus Outnuts

Pro	gramm	ed Atti	enuatio	n Inpu	t	OUTPUT	L	ogic A	ssembly	Outp	ut
Decimal		2-	Digit B	CD		RANGE					Over- range
(dB)	100	80	40	20	10	(dBm)	80 L	40L	20 L	10 L	10H
0	L	L	L	L	L	+10	L	L	L	L	Н
10	L	L	L	L	Н	0	L	L.	L	L	L
20	L	L	L	Н	L	-10	L	L	L	Н	L
30	L	L	L	Н	Н	-20	L	L	Н	L	L
40	L	L	Н	L	L	-30	L	Ł	Н	Н	Ł
50	L	L	Н	L	Н	-40	L	Н	L	L	L
60	L.	L	Н	Н	L	-50	L	Н	L	Н	L
70	L	L	Н	Н	Н	-60	£	Н	Н	L	L
80	L	н	L	L	L	-70	L	Н	Н	Н	L
90	L	Н	L	L	Н	-80	н	L.	L	L	L
100	Н	L	L	L	L	-90	Н	L	L	Н	L
110	H	L	L	L	Н	-100	Н	L	Н	Ĺ	L
120	Н	L	L	Н	L	-110	н	L	Н	Н	L
130	Н	L	L	Н	Н	-120	Н	Н	L	L	L
140	н	L	Н	L	L	-130	н	Н	L	Н	L
150*	н	L	Н	L	н	-140*	н	Н	Н	L	Ł

For safety purposes, the shift registers are set for 150 dB attenuation upon initiation the remote mode of operation.

BCD-To-Binary Converter

	Ir	put		Output			
100	80	40	20	80	40	20	
L	L	L	L	L	L	L	
L	L	L	Н	L	L	Н	
L	L	H	L	L	Н	L	
L	L	H	H	L	H	H	
L	Н	L	L	Н	L	L	
Н	L	L	L	Н	L	H	
Н	L	L	Н	Н	Н	L	
Н	L	H	L	Н	Н	Н	

A21 Filter Driver Assembly

SERVICE SHEET 10

Service Model 86603A

SERVICE SHEET 11 (Cont'd)

Full Adder

			nputs		Outputs				
A ₄	A ₃	A ₂	A ₁	C ₀ , B ₂ , B ₃ , B ₄	Σ4	Σ3	Σ2	Σ1	
80	40	20	10	Over-range	80	40	20	10	
L	L	L	L	L	L	L	L	L	
L	L	L	H	H	L	L	L	L	
L	L	H	L	H	L	L	L	H	
L	L	H	H	H	L	L	H	L	
L	H	L	L	H	L	L	Н	H	
L	H	L	H	H	L	H	L	L	
L	H	H	L	H	L	H	L	H	
L	H	H	H	H	L	H	H	L	
H	L	L	L	H	L	H	Н	H	
H	L	L	H	H	H	L	L	L	
H	L	H	L	H	H	L	L	H	
H	L	H	H	H	H	L	H	L	
H	H	L	L	H	H	L	Н	H	
H	H	L	H	H	H	H	L	L	
H	H	H	L	H	H	H	L	H	
H	H	H	H	H	Н	H	H	L	

Local Remote Multiplex

The LCL/RMT input is a logic low in the remote mode. This enables the gates which are connected to the remote attenuation inputs (Full Adder and Over-range) so the remote signals drive the 10 dB Step Attenuator. At the same time logic inputs from the OUTPUT RANGE switch are inhibited.

TROUBLESHOOTING

It is assumed that the troubleshooting information on Service Sheet 3 was used to isolate a circuit defect to the assembly shown on the accompanying diagram. Troubleshoot the Logic Assembly by using the test equipment and procedures given below.

Test Equipment
Digital Voltmeter . . . HP 3466A

If the problem is evident only in the local mode of operation, check the OUTPUT RANGE switch, continuity of the connections to the A11 assembly, and the Local/Remote Multiplexer. Refer to

an associated component is probably defective. $\label{eq:note} \textbf{NOTE}$

the table showing the OUTPUT RANGE switch

output. If the defect is evident only in the remote

mode of operation, check the shift registers, the

BCD-to-Binary Decoder the Full Adder and the

Use the tables showing inputs versus outputs as a

If the defect is evident in both the Local and

Remote modes, the Local/Remote Multiplexer or

tool to isolate the defective component.

Local/Remote Multiplexer for proper operation

If the inputs and outputs of the A11 Logic Assembly are correct, check the 10 dB Step Attenuator (Service Sheet 6) in all ranges, the 10 dB Attenuator in the A4 Detector Amplifier Assembly, and the 1 dB Step Attenuator in the A10 feeter assembly (also the 10H inputs and associated components). Also, check the 1 dB and 10 dB Step Attenuator outputs with attenuation inputs of 1, 2, 4, and 8 dB and 10, 20, 40, and 80 dB.

8-40

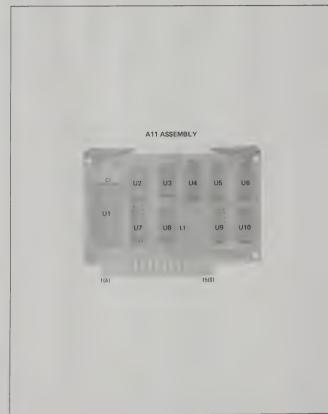


Figure 8-29. A11 Logic Assembly Component Locations

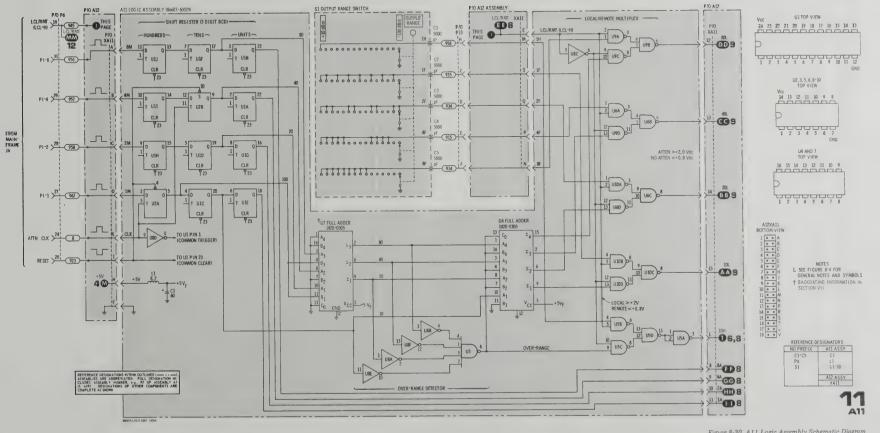


Figure 8-30. A11 Logic Assembly Schematic Diagram

Service Model 86603A

SERVICE SHEET 12 (Cont'd)

Front panel operation (local mode) is enabled by a high input (>+2.0 Vdc) on the LCL/RMT line. (The NC mnemonic at A23U1A pin 2 indicates no connection which ensures an equivalent high input for this particular integrated circuit.) Pressing the FREQ DOUBLER switch passes the low output to A23U1D. In LCL mode the input to A23U1D pin 12 is always high. Therefore, the output of A23U1D goes high which biases A23Q1 on and DS1 (which indicates the frequency doubling mode) is illuminated. The low output from A23U1C is coupled through A24CR3 to the DBL-L input of the A20 assembly.

When the remote control mode is initiated, a low input appears on the LCL/RMT line. This action inhibits the front panel switch control of the DBL-L output while enabling remote control by ensuring that a high input always occurs at A23U1D pin 13. The DBL-L input from the mainframe now governs the lamp indication and the A20 Assembly DBL-L input.

If an option 003 RF Section is used with an 8660C mainframe, the Frequency Doubler Test Switch must be placed in the 8660C position. Front panel control of doubling is inhibited by the low input to A23U1A through A24CR2. A24CR1 isolates the LCL/RMT control line from the grounded input. The open (high) input to A23U1D pin 12 ensures that the front panel lamp remains off. A24CR3

isolates the output of A23U1C from the DBL-L input from the mainframe to the A20 Assembly.

TROUBLESHOOTING

It is assumed that the troubleshooting information in Service Sheet 3 was used to isolate a circuit defect to the circuits represented on the schematic. Troubleshoot the circuits using the test equipment and information which follows.

Test Equipment

Digital Voltmeter. HP 3466A

Before troubleshooting the circuit boards shown by the schematic, verify that the power supply inputs to the circuit boards are all correct.

The logic levels should not change unless a change in center frequency is made. Check the outputs and inputs of the A20 Assembly against the levels shown by the table. If the inputs are correct the defect is in the A20 Assembly circuitry. One or more incorrect outputs will isolate the defective stage. If the inputs are incorrect, a defective switch, diode, or wiring is responsible. In option 003 instruments, the time to isolate the defect may be reduced by using the Frequency Doubler Test Switch. If necessary, point-by-point measurements of voltage will aid quick identification of a defective stage and/or component.

DOUBLE! AMPLIFIE CONTRO!

CODE

DISASSEMBLY AND INTERCONNECTION PROCEDURES (Cont'd)

b. Make connection from J6 (mainframe) to P6 (RF Section rear panel) with the 11672-60001 multi-pin interconnect cable.

WARNING

To avoid contact with the line voltage, remove the line (main) power cable from the power outlet before removing or connecting cables to the Frequency Extension Module.

- c. Connect the 1250-1236 adapter to the 11672-60005 gray coaxial cable. Insert the adapter into P2 (on RF Section rear panel above the multipin connector).
- d. Remove the gray-blue cable from the jack on the rear side of the Frequency Extension Module. Connect the gray coaxial cable to the extension module jack.
- e. Take the 11672-60004 red coaxial cable and connect it to P1 (RF Section rear panel below the multi-pin connector).
- f. Disconnect the gray cable from the other extension module output jack. Connect the red coaxial cable to the jack.
- g. Reconnect the mainframe line (Main) power cable to the power outlet and set the mainframe line switch to ON.

Installation and Reassembly Procedures

To reinstall the RF Section covers, follow the procedure steps in reverse order. Be sure the cover notches are to the rear. Instructions for installing the RF Section into the mainframe may be found in Section II.

After troubleshooting, be sure the Frequency Extension Module output cables are connected to the correct output jacks by following the interconnection procedure steps in the reverse order.

NOTE

When a malfunction occurs, refer to Section VIII of the HP Model 8660-series mainframe Operating and Service Manual to begin troubleshooting (System Troubleshooting Guide), If that information indicates possible problems in the RF Section, refer to the Systems Troubleshooting information in Service Sheet 1. This information may be used to isolate the defect to the RF Section, another plug-in, or the mainframe, If the problem is in this plug-in, return to Service Sheet 2 for further troubleshooting information.

PRINCIPLES OF OPERATION

General

The system center frequency controls the RF Section's frequency doubling mode and the ALC loop bandwidth. This is accomplished by means of the DBL-L and Code 1 logic inputs which are connected from the mainframe DCU to the A20 Doubler Power Supply Assembly in the RF Section.

In Option 003 RF Sections, the DBL-L input may be controlled from the front panel. This allows frequency doubling with Models 8660A and 8660B mainframes (Frequency Doubler Test Switch A24S1 is set to the 8660A/B position). In modified A and B mainframes, remote control of frequency doubling is possible. (Refer to the paragraph entitled Required Modifications in Section I.)

When the option 003 RF Section is used in an 8660C mainframe (A24S1 is set to the 8660C position), front panel control of frequency doubling is inhibited. The doubling mode is automatically entered whenever center frequencies ≥1300 MHz are selected. This occurs in both the local or remote control modes.

The OP-1 and OP-2 outputs to the mainframe serve to identify the RF Section model to the mainframe DCU. This information allows proper response of the mainframe frequency limiting logic circuits.

A20 Doubler Power Supply Assembly

The DBL-L and Code 1 inputs to the A20 Assembly control the frequency doubling mode and ALC loop bandwidth. The DBL-L exerts direct control over the Doubler Amplifiers and Doubler Relay Control outputs. Both inputs influence the ALC Bandwidth Control output. The following table lists pertinent center frequencies with the resulting A20 Assembly inputs and outputs.

+24V Regulator. In the frequency doubling mode, the Doubler Amplifiers Control output is +22 Vdc. A20U1 is a self contained voltage regulator. The +22V Adj, A20R7 controls the amount of voltage feedback to the regulator and therefore sets the output voltage. A20Q1 is an external transistor which drives the series pass transistor Q1.

SERVICE SHEET 12 (Cont'd)

A 20 Assembly Inputs and Outputs

0	Inputs		Control Outputs		
Center Frequency	DBL-L	Code 1	Doubler Amplifiers	ALC BW	Doubler Relay
<10 MHz	Н	Н	0 Vdc	>+4.0 Vdc	0 Vdc
≥10 MHz but <1300 MHz	Н	L	0 Vdc	<+0.3 Vdc	0 Vdc
≤1300 MHz	L	L	+22 Vdc	>+4.0 Vdc	+12 Vdc
H = >+2.0 Vdc	L = <	-0.8 Vdc			

Power Supply Switch. When A20Q2 is biased "on," the drive current to the regulator transistors (both internal and external to A20U1) is removed. This causes the regulator output to go to ground potential. This occurs only with the DBL-L input high (>+2.0 Vdc).

Relay Driver. When the system is operating in the frequency doubling mode, the DBL-L input is low. Therefore, A20Q3 is biased off, A20Q4 is biased on, and approximately +12 Vdc appears at the Doubler Relay Control output.

ALC Bandwidth Control. At center frequencies <10 MHz, the Code 1 input is high. A20Q5 is biased on, A20Q6 is biased off, and the ALC BW Control output increases until it is limited by A20VR2 (≈+5 Vdc). At center frequencies ≥1300 MHz, the override voltage from the Doubler Relay Control output (connected to A20Q5 through A20CR2 and A20R16) cancels the effect of the Code 1 low input. The ALC BW Control again increases to ≈+5 Vdc.

Frequency Doubler Test Switch (Except Option 003 Instruments)

When used in an 8660C mainframe, the Frequency Doubler Test Switch S1 should be left in the 8660C position. The other two switch positions are strictly for test purposes. The diode CR1 isolates the DBL-L input from ground in the 8660A/B X2 position.

The grounded OP-2 output (in the 8660C position of S2) indicates to the mainframe DCU that the Center frequency limit of the RF Section is 2600 MHz. In the other positions, a limit of 1300 MHz is indicated by the grounded OP-1 output.

Option 003 Instruments

Option 003 instruments are intended to be used with 8660A or 8660B mainframes to provide the frequency doubling capability. The Frequency Doubler Test Switch, A24S1 should be set to the 8660A/B position. The OP-1 output to the mainframe is grounded indicating a maximum frequency of 1300 MHz. In the doubling mode, the mainframe center frequency readout indicates one-half the actual output frequency.

SERVICE SHEET 12 (Cont'd)

Front panel operation (local mode) is enabled by a isolates the output of A23U1C from the DBL-L high input (>+2.0 Vdc) on the LCL/RMT line. input from the mainframe to the A20 Assembly. (The NC mnemonic at A23U1A pin 2 indicates no connection which ensures an equivalent high input TROUBLESHOOTING for this particular integrated circuit.) Pressing the FREQ DOUBLER switch passes the low output to A23U1D. In LCL mode the input to A23U1D pin 12 is always high. Therefore, the output of A23U1D goes high which biases A23Q1 on and DS1 (which indicates the frequency doubling mode) is illuminated. The low output from A23U1C is coupled through A24CR3 to the DBL-L input of the A20 assembly.

input appears on the LCL/RMT line. This action by the schematic, verify that the power supply inhibits the front panel switch control of the inputs to the circuit boards are all correct. DBL-L output while enabling remote control by ensuring that a high input always occurs at The logic levels should not change unless a change A23U1D pin 13. The DBL-L input from the in center frequency is made. Check the outputs mainframe now governs the lamp indication and and inputs of the A20 Assembly against the levels the A20 Assembly DBL-L input.

mainframe, the Frequency Doubler Test Switch stage. If the inputs are incorrect, a defective must be placed in the 8660C position. Front panel switch, diode, or wiring is responsible. In option control of doubling is inhibited by the low input to 003 instruments, the time to isolate the defect may A23U1A through A24CR2. A24CR1 isolates the be reduced by using the Frequency Doubler Test LCL/RMT control line from the grounded input. Switch. If necessary, point-by-point measurements The open (high) input to A23U1D pin 12 ensures of voltage will aid quick identification of a that the front panel lamp remains off, A24CR3 defective stage and/or component.

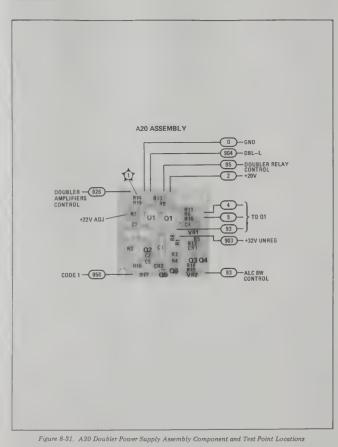
It is assumed that the troubleshooting information in Service Sheet 3 was used to isolate a circuit defect to the circuits represented on the schematic. Troubleshoot the circuits using the test equipment and information which follows.

Digital Voltmeter. HP 3466A

When the remote control mode is initiated, a low Before troubleshooting the circuit boards shown

shown by the table. If the inputs are correct the defect is in the A20 Assembly circuitry. One or If an option 003 RF Section is used with an 8660C more incorrect outputs will isolate the defective

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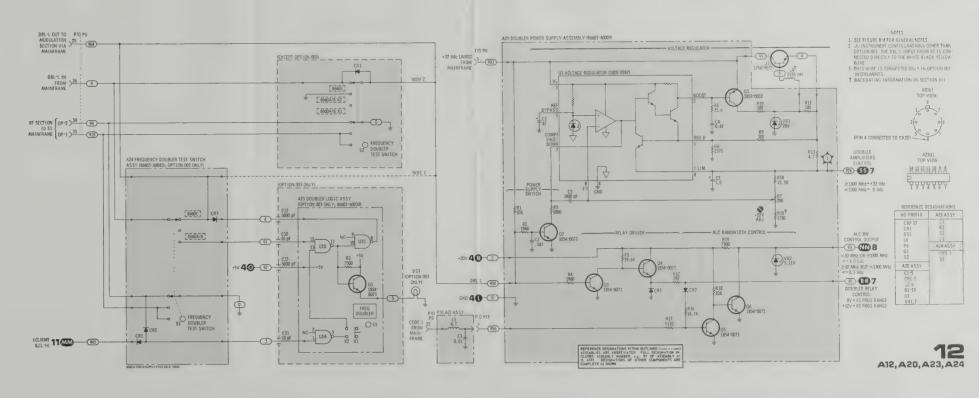


Figure 8-32. A20 Doubler Power Supply and Option 003 Circuits Schematic Diagram

Service

Table 8-2. Assemblies, Chassis Mounted Parts, and Adjustable Component Locations (1 of 2)

Reference Designator	Service Sheets	Figures	Remarks
A1 Assembly	2, 4	_	Circuit Board, mounted on aluminum decl opposite the A5 Assembly.
A2 Assembly	2, 4, 8	8-22, 33	A3, A4, and A16 plug into connectors mounted on A2.
A3 Assembly A3R4 ADJ, LIN	2, 8 8	8-20, 33 8-20, 33	8-33, Top View
A4 Assembly A4R13 ADJ, DET BIAS A4R26 ADJ, MTR BIAS A4S1 SWITCH, TEST/NORMAL	2, 6 6 6 2, 6	8-16, 33 8-16, 33 8-16, 33 8-16, 33	8-33, Top View 8-33, Top View 8-33, Top View
A5 Assembly A6 Assembly A7 Assembly A8 Assembly A9 Assembly	2, 4 2, 6 2, 4 2, 4 3, 9	8-33 8-33 8-11, 33 8-33 8-24, 33	8-33, Top View 8-33, Left Side View
A10 Assembly A10R2 ADJ, AM LIN A10R5 ADJ, AM CAL A10R7 ADJ, RF LEVEL	2, 8 8 8 8	8-21, 33 8-21, 33 8-21, 33 8-21, 33	8-33, Left Side View 8-33, Top View 8-33, Top View 8-33, Top View
A11 Assembly A12 Assembly	3, 11 2, 4	8-29, 33 8-33	8-13, Left Side View (A9, A10, and A11 plug into connectors mounted on A12)
A13 Assembly A14 Assembly A15 Assembly	2, 9 — 2, 4	8-33 8-33 8-33	Wiring harness Rear Panel Internal
A16 Assembly A16C8 ADJ, FREQ RESP A16R1 ADJ, THIRD HARM A16R2 ADJ, GAIN	2,5 5 5 5	8-13, 33 8-13 8-13, 33 8-13, 33	8-33, Top View 8-33, Top View 8-33, Top View
A16R3 ADJ, SECOND HARM A16R4 ADJ, GAIN TRACKING	5 5	8-13, 33 8-13, 33	8-33, Top View 8-33, Left Side View
A17 Assembly A18 Assembly A19 Assembly	2, 5 2, 5 2, 5	8-14, 33 8-33 8-33	
A20 Assembly A20R7, ADJ, +24V	3, 12 12	8-31, 33 8-31, 33	8-33, Top View 8-33, Top View
A21 Assembly A22 Assembly A23 Assembly	3, 10 2, 7 12	8-27, 33 8-18, 33	Not Shown (mounted in front panel housing; Option 003 only)
A24 Assembly	12		Not Shown (replaces S2 in Option 003 only).
AT1 AT2	4 5	8-33	Not Shown, connected at A8 input
C1-5 C6 C7	3, 11 2, 6 2, 8	8-33 8-33 8-33	8-33 Left Side View Insert 8-33 Left Side View Insert 8-33 Left Side View Insert Mounted on TR1 (see 8.33 Top View)
C8, 9 C10-13	6 12	8-33	Mounted on TB1 (see 8-33 Top View) 8-33 Left Side View Insert

Table 8-2. As

	1 uoie 0-2.	AS
R	eference	Desi
CR1		
DS1		
FL1		
J1		
L1, 2		
M1		
P1, 2		
P3, 4		
P5		
P6		
P7		
P13		
P14		
Q1		
R1		
R2		
S1		
S2		
TB1		
W1*		
W2* W3		
W4*		
W5*		
W6*		
W7*		
W8		
W9		
W10*		
W11		
W12		
W13*		
W14		
W15		
W16		
W17 W18		
W19 W20		
W20 W21		
XA21		
	-4	
Tindic	ates semi-ri	gid c

Disassembly and Interconnection Procedures Assemblies, Chassis Mounted Parts, and Adjustable Component Locations.

b. Make connection from J6 (mainframe) to P6 (RF Section

rear panel) with the 11672-60001 multi-pin interconnect cable.

WARNING

To avoid contact with the line voltage, remove the line (main) power cable from the power outlet before removing or connecting cables to the Frequency Extension Module.

c. Connect the 1250-1236 adapter to the 11672-60005 gray coaxial cable. Insert the adapter into P2 (on RF Section rear panel above the multipin connector).

d. Remove the gray-blue cable from the jack on the rear side of the Frequency Extension Module. Connect the gray coaxial cable to the extension module jack.

e. Take the 11672-60004 red coaxial cable and connect it to P1 (RF Section rear panel below the multi-pin connector).

f. Disconnect the gray cable from the other extension module output lack. Connect the red coaxial cable to the lack.

g. Reconnect the mainframe line (Main) power cable to the power outlet and set the mainframe line switch to ON.

Installation and Reassembly Procedures

To reinstall the RF Section covers, follow the procedure steps in reverse order. Be sure the cover notches are to the rear. Instructions for installing the RF Section into the mainframe may be found in

After troubleshooting, be sure the Frequency Extension Module output cables are connected to the correct output jacks by following the interconnection procedure steps in the reverse order.

> A20 Doubler Power Supply Assembly A23 Doubler Logic SERVICE SHEET 12

DISASSEMBLY AND INTERCONNECTION PROCEDURES (Cont'd)

CAUTION

Before removing the RF Section plug-in from the mainframe, remove the line (Mains) voltage by disconnecting the power cable from the power

RF Section Plug-in Removal

a. Release the latch below the front panel OUTPUT jack.

b. Pull the latch out while rotating it to the left until it is perpendicular to the front panel. This separates the mating plug and jack (plug-in to mainframe).

c. Grasp the latch and pull the plug-in straight out from mainframe

Plug-in Cover Removal

a. Remove the 16 pozidriv screws from both covers.

b. Loosen the 4 screws which hold the teflon/aluminum plug-in guide in place.

c. Remove the covers and set them aside

d. If necessary, remove the plug-in guides by removing the screws.

Interconnection of RF Section to Mainframe for Troubleshooting

After the RF Section is removed from the mainframe and its covers have been removed, the RF Section must be reconnected to the mainframe with interconnecting extender cables before troubleshooting can begin.

WARNING

With the mainframe top cover removed, power is supplied to the system during troubleshooting, Energy available at many points may, if contacted. constitute a shock hazard.

a. Remove the mainframe top cover. First remove the 4 Pozidriv screws; then slide the cover back and off the mainframe siderails.

NOTE

The interconnect cables and adapters are parts found in the HP 11672A Service Kit, They may all be ordered in the kit or as individual pieces. Refer to the 11672A Operating Note for a pictorial cross reference.

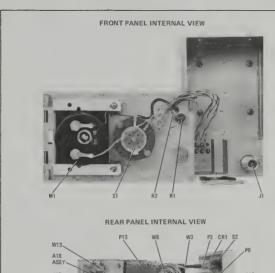
Service Model 86603 A

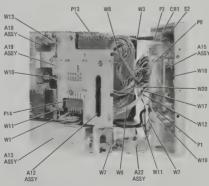
Table 8-2. Assemblies, Chassis Mounted Parts, and Adjustable Component Locations (1 of 2)

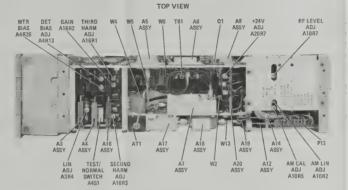
Reference Designator	Service Sheets	Figures	Remarks
A1 Assembly	2, 4	-	Circuit Board, mounted on aluminum of opposite the A5 Assembly.
A2 Assembly	2, 4, 8	8-22, 33	A3, A4, and A16 plug into connectors mounted on A2.
A3 Assembly A3R4 ADJ, LIN	2, 8 8	8-20, 33 8-20, 33	8-33, Top View
A4 Assembly A4R13 ADJ, DET BIAS A4R26 ADJ, MTR BIAS A4S1 SWITCH, TEST/NORMAL	2, 6 6 6 2, 6	8-16, 33 8-16, 33 8-16, 33 8-16, 33	8-33, Top View 8-33, Top View 8-33, Top View
A5 Assembly A6 Assembly A7 Assembly A8 Assembly A9 Assembly	2, 4 2, 6 2, 4 2, 4 3, 9	8-33 8-33 8-11, 33 8-33 8-24, 33	8-33, Top View
A10 Assembly A10R2 ADJ, AM LIN A10R5 ADJ, AM CAL A10R7 ADJ, RF LEVEL	2, 8 8 8 8 8	8-21, 33 8-21, 33 8-21, 33 8-21, 33	8-33, Left Side View 8-33, Top View 8-33, Top View 8-33, Top View
A11 Assembly A12 Assembly	2, 4	8-29, 33 8-33	8-13, Left Side View (A9, A10, and A11 plug into connector mounted on A12)
A13 Assembly A14 Assembly A15 Assembly	2, 9 - 2, 4	8-33 8-33 8-33	Wiring harness Rear Panel Internal
A16 Assembly A16C8 ADJ, FREQ RESP A16R1 ADJ, THIRD HARM A16R2 ADJ, GAIN	2,5 5 5 5	8-13, 33 8-13 8-13, 33 8-13, 33	8-33, Top View 8-33, Top View 8-33, Top View
A16R3 ADJ, SECOND HARM A16R4 ADJ, GAIN TRACKING	5	8-13, 33 8-13, 33	8-33, Top View 8-33, Left Side View
A17 Assembly A18 Assembly A19 Assembly	2, 5 2, 5 2, 5	8-14, 33 8-33 8-33	
A20 Assembly A20R7, ADJ, +24V A21 Assembly	3, 12 12	8-31, 33 8-31, 33	8-33, Top View 8-33, Top View
A22 Assembly A23 Assembly	3, 10 2, 7 12	8-27, 33 8-18, 33	Not Shown (mounted in front panel housing; Option 003 only)
A24 Assembly	12		Not Shown (replaces S2 in Option 003 only).
AT1 AT2	4 5	8-33	Not Shown, connected at A8 input
C1-5 C6 C7 C8, 9	3, 11 2, 6 2, 8 6	8-33 8-33 8-33	8-33 Left Side View Insert 8-33 Left Side View Insert 8-33 Left Side View Insert Mounted on TB1 (see 8-33 Top View)
C10-13	12	8-33	8-33 Left Side View Insert

Table 8-2. Assemblies, Chassis Mounted Parts, and Adjustable Component Locations (2 of 2)

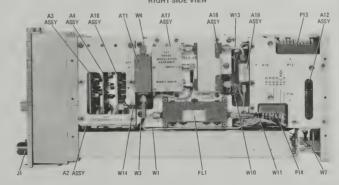
Reference Designator	Service Sheets	Figures	Remarks
CR1 DS1 FL1 J1	3, 12 12 2, 4	8-33 3-2 8-33 8-33	8-33 Rear Panel Option 003 instruments only 8-33 Right Side View
L1, 2	6	0.00	Mounted on TB1 (see 8-33 Top View)
M1	2, 6	8-33	8-33 Front Panel Internal
P1, 2 P3, 4 P5 P6	2, 4 6 4 2, 3, 4, 5, 8-12	3-3, 8-33	3-3, P2 is ①: P1 is ② Not shown, +20V inputs to A6. Not shown, +20V input to A8 3-3, P6 is ③
P7 P13 P14	2, 4, 6, 8, 9 2, 6, 9	8-33 8-33	Not shown, -10V input to A8
R1 R2	2, 8 8	8-33 8-33 8-33	8-33, Front Panel Internal View 8-33, Front Panel Internal View
S1 S2	3, 11 3, 12	8-33 8-33	8-33, Front Panel Internal View 8-33, Rear Panel Internal View
TB1	6	8-33	Top View
W1* W2* W3 W4* W5*	2, 5 2, 4 2, 4 2, 4 2, 4	8-33 8-33 8-33 8-33 8-33	Right Side View, FL1 Output Top View A8, Output AT1 Input, grey/blue AT1 Output Top View, A5 Output
W6* W7* W8 W9 W10*	2, 4, 6 2, 7, 9 2, 8 2, 8 2, 5	8-33 8-33 8-33 8-5, 33 8-33	Top View, A6 Input A13 Input AM Inpt to A12, grey/yellow Pulse Inpt to A12, white/green A18 Output
W11 W12 W13* W14	2, 4 2, 5 2, 4, 5 2, 5	8-33 8-5, 33 8-33 8-33	FL1 Input, grey
W15 W16 W17 W18	2, 6, 7 2, 7 2, 4 2, 4	8-33 8-33 8-33 8-33	Black, A22 Input Black, A22 Interconnect P6 Interconnect cable, white/brown A15 Output to P6, white/red
W19 W20 W21	2, 4 2, 4 2, 4	8-33 8-33 8-33	A15 Input from P6, white/blue P6 Interconnect cable, white/orange P6 Interconnect cable, white/yellow
XA21	10	-	Printed Circuit connector for A21.

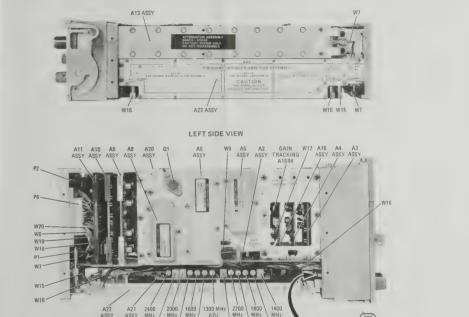






RIGHT SIDE VIEW





A21 ADJ

A21 FINE ADJ

BOTTOM VIEW

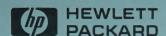
Figure 8-33. Assemblies, Chassis Parts, and Adjustable Component Locations



HEWLETT PACKARD

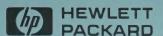
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COMPANY	
ADDRESS	
TECHNICAL CONT	FACT PERSON
PHONE NO.	EXT.
MODEL NO.	SERIAL NO.
MODEL NO.	SERIAL NO.
P.O. NO.	DATE
Accessories returned	d with unit
NONE	□ CABLE(S)
POWER CABLE	□ADAPTER(S)
OTHER	
	over



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Accessories returned	d with unit
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□ POWER CABLE	□ADAPTER(S)
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MODEL NO.	SERIAL NO.
P.O. NO.	DATE
Accessories returne	ed with unit
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POWER CABLE	□ ADAPTER(S)
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MODEL NO.	SERIAL NO.
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Accessories returne	d with unit
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POWER CABLE	□ ADAPTER(S)
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MODEL NO.	SERIAL NO.
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COMPANY

Should one of your HP instruments need repair, the HP service organization is ready to serve you. However, you can help us serve you more effectively. When sending an instrument to HP for repair, please fill out this card and attach it to the product. Increased repair efficiency and reduced turn-around time should result.

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MODEL NO.	SERIAL NO.
2.0. NO.	DATE
Accessories returne	d with unit
INONE	☐ CABLE(S)
POWER CABLE	□ ADAPTER(S)
THER	

Service needed	Service needed	Service needed
CALIBRATION ONLY	CALIBRATION ONLY	CALIBRATION ONLY
☐ REPAIR & CAL	☐ REPAIR ☐ REPAIR & CAL	☐REPAIR ☐ REPAIR & CAL
OTHER	OTHER	OTHER
Observed symptoms/problems	Observed symptoms/problems	Observed symptoms/problems
FAILURE MODE IS:	FAILURE MODE IS:	FAILURE MODE IS:
CONSTANT DINTERMITTENT	CONSTANT INTERMITTENT	CONSTANT DINTERMITTENT
SENSITIVE TO:	SENSITIVE TO:	SENSITIVE TO:
COLD HEAT VIBRATION	□ COLD □ HEAT □ VIBRATION	☐ COLD ☐ HEAT ☐ VIBRATION
FAILURE SYMPTOMS/SPECIAL	FAILURE SYMPTOMS/SPECIAL	FAILURE SYMPTOMS/SPECIAL
CONTROL SETTINGS	CONTROL SETTINGS	CONTROL SETTINGS
If unit is part of system list model	If unit is part of system list model	If unit is part of system list model
number(s) of other interconnected in- struments.	number(s) of other interconnected in- struments.	number(s) of other interconnected in- struments.
9320-3896 Printed in U.S.A.	9320-3896 Printed in U.S.A.	9320-3896 Printed in U.S.A.
Service needed	Service needed	Convine needed
	Service needed	Service needed
☐ CALIBRATION ONLY ☐ REPAIR ♣ CAL	☐ CALIBRATION ONLY ☐ REPAIR ☐ REPAIR & CAL	☐ CALIBRATION ONLY ☐ REPAIR ☐ REPAIR & CAL
	E KETAIN & GAL	
OTHER	OTHER	OTHER
Observed symptoms/problems	Observed symptoms/problems	Observed symptoms/problems
FAILURE MODE IS:	FAILURE MODE IS:	FAILURE MODE IS:
CONSTANT DINTERMITTENT	CONSTANT DINTERMITTENT	CONSTANT INTERMITTENT
SENSITIVE TO:	SENSITIVE TO:	SENSITIVE TO:
□ COLD □ HEAT □ VIBRATION	□ COLD □ HEAT □ VIBRATION	☐ COLD ☐ HEAT ☐ VIBRATION
FAILURE SYMPTOMS/SPECIAL	FAILURE SYMPTOMS/SPECIAL	FAILURE SYMPTOMS/SPECIAL
CONTROL SETTINGS	CONTROL SETTINGS	CONTROL SETTINGS
		25
If unit is part of system list model number(s) of other interconnected instruments.	If unit is part of system list model number(s) of other interconnected instruments.	If unit is part of system list model number(s) of other interconnected instruments.
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